μ-COMP DDP-416 General Purpose I/C Digital Computer

Honeywell

COMPUTER CONTROL
DIVISION

FEATURES

16-bit; all silicon monolithic integrated circuits

Fully parallel machine organization

16-bit word, two's complement

960 nanosecond memory cycle time

4096-word μ-**STORE** ICM-40 magnetic core memory

Memory expansion to 16,384 words in standard cabinet

Multi-level indirect addressing

Large sector size for maximum memory efficiency

Direct addressing of full memory with DESEC-TORIZING software

Simple command format; comprehensive instruction repertoire

Most instructions executed in 1.92 μsecs or less

Priority interrupt standard

Power failure interrupt standard

Memory lockout option for program protection

Memory parity option

Real-time clock option

I/O designed for real-time systems interface

Individually buffered I/O devices

Two-cycle I/O commands select device, test status, and transfer data

No I/O hold-off

Flexible priority scheme with program settable masks

DMC option for economical time-shared I/O

Direct memory access option for mc I/O rates

ASR-33 or ASR-35 option

Selectable one- or two-pass assembler

Desectorizing loader

Bootstrap loader protected in read-only memory

Fixed point subroutine library

Compact mechanical packaging

Movable control console

Front access for ease of maintenance

Modular plug-in options for easy expansion

Full line of compatible I/C modules and accessories available for systems designer

Price: upon request

Liberal OEM terms available

INTRODUCTION & GENERAL DESCRIPTION

Tomorrow's breed of I/C computer today . . . and at off-the-shelf price

The μ-**COMP** DDP-416 general purpose digital computer offers a price/performance ratio that can't be beat: full size 16-bit capability, nano-second speeds, I/C size/reliability, ASCII compatibility, wide instruction repertoire and simple memory addressing.

The DDP-416 is the third member of 3C's growing μ-**COMP** family of I/C computers . . . and our third 16-bit system to date. It is backed by a dozen successful years in the digital electronics industry, by programming and maintenance courses conducted by 3C experts, by an active computer users' group and by the continuing support of Honeywell.

Modular design, flexible I/O structure and powerful command repertoire enable the DDP-416 to meet a broad variety of applications wherever real-time performance characteristics are the major criteria.

General characteristics include fully parallel organization, multi-level indirect addressing, powerful I/O system, 30-command instruction repertoire and straightforward logic for easy system interface and field expansion.

Standard DDP-416 hardware provides direct addressing to 1024 words of core memory with a single command. This capability is extended by DESECTORIZING, an important software feature that allows the programmer to directly address the entire memory without considering sector boundaries. This software generates indirect address linkages when crossing sector boundaries as necessary . . . redundant linkages are never generated. Thus, a program written in assembly language will, in general, be more efficient than a program written by the programmer who must be concerned with indirect address linkages.

Software package includes such DDP-116 proven programs as utility routines, arithmetic subroutine library, I/O library, and DEBUG (DDP-416 debugging aid). DAP-16 (DDP-416 assembly program), is unique in that it allows the operator to specify a one- or two-pass assembly for the same source program; one-pass being preferable for the basic system, two pass for systems with high speed input devices where more detailed listings are desired. The one- and two-pass options allow the programmer to directly address all of memory in his source program through the use of DESECTORIZING software. More than 50 programs are available. All DDP-416 programs are compatible with other 3C 16-bit computers and thus can be run on either the DDP-116 or DDP-516.

The DDP-416 features compact mechanical packaging, ideal for implementation into complex systems configurations — fits into a standard 19-inch rack and takes less than 36 inches of vertical rack space. Its movable control console is designed to allow complete operator freedom. Vertical leaves, which tilt out for easy front access to both modules and interwiring, house the central processor (with ample space for optional additions) and the μ-**STORE** ICM-40 core memory (with space for up to 16,384 words).

BACKGROUND
Our third 16-bit system; our third I/C computer

Computer Control has, for more than twelve years, set the pace in the digital computer/digital systems industry as a leading manufacturer of digital modules, core memories, and general purpose computers. 3C was among the first to recognize integrated circuit technology as the key to future growth: the first to offer a complete I/C digital logic line after two years of in-house funded research and development. And the first to offer a commercial I/C computer. This technological strength, coupled with 3C's 16-bit hardware and software development experience and Honeywell corporate resources, gives the *μ-COMP* DDP-416 user more computer for the money than any other system available today.

μ-PAC I/C Digital Logic Modules — The *μ-PAC* I/C modules used as basic building blocks in the *μ-COMP* DDP-416 are the result of extensive in-house research at 3C's Advanced Techniques Laboratory. They bring to the DDP-416 system high reliability, low cost per logic function, speed and ease of maintenance. Rigid inspection, test and over-all quality assurance programs are an integral part of both *μ-PAC* and *μ-COMP* DDP-416 manufacturing processes.
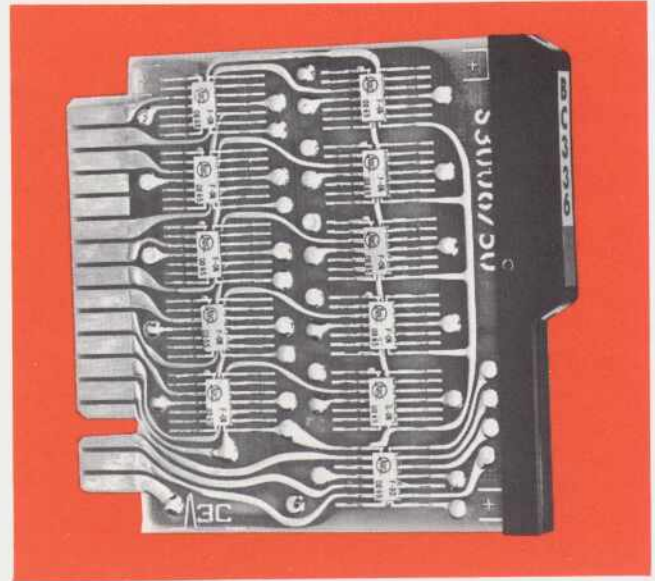
ICM-40 Core Memory — This compact, high speed *μ-STORE* system, field-proven in a variety of installations including the DDP-124 and DDP-516 general purpose computers, is the heart of the *μ-COMP* DDP-416. *μ-PAC* I/C modules are used throughout. This is the same high speed memory system sold by 3C as a standard product.

DDP-124 — Introduced in 1965, this machine was the first truly I/C computer commercially available. Features proven in the *μ-COMP* DDP-124 and found in the DDP-416 include automatically wired back planes mounted vertically in swing-out drawers for easy access to both PACS and wiring, built-in cooling fans, cable PAC connectors for easy interface and expansions, plus the same *μ-PAC* logic and the same ICM-40 type memory. Proven production capabilities insure quick delivery and reliable performance of the DDP-416.

DDP-116 — First 16-bit computer to be announced . . . first to be delivered . . . the DDP-116 has gained a wealth of experience in well over 125 installations in industry, in the military, in research, and in numerous other real-time environments. This background in unmatched by any 16-bit system offered today.

DDP-516 — Program compatible with the DDP-416, this 16-bit system features a 72-instruction repertoire and greater memory expandability. DDP-516 and DDP-416 were specifically engineered to meet a wide variety of application needs with hardware and software designed to offer a range of capability at the lowest possible cost.

SPECIFICATIONS
Engineered for maximum performance at lowest cost

Type
16-bit parallel binary
Two's complement arithmetic
Coincident-current random-access ferrite core memory, 4K to 16K
Single address with multi-level indirect addressing

Speed
Memory cycle time	960.	nsec
Add	1.92	μsec
Subtract	1.92	μsec
Single word I/O transfer	1.92	μsec

Time multiplex I/O transfer: 260 kc with DMC*
Over 1 mc with DMA*

Power
1 kw at 115 vac $\pm10\%$, 60 ±2 cps single phase
Power failure interrupt is standard

Weight
250 lbs.

Temperature
0° to 45°C (32° to 113°F)
(Central processor less any I/O devices)

Dimensions (without console)
24" x 24" x 38"

Cooling
Filtered, forced air cooling provided within central processor cabinet

Signal Levels
Logic ZERO: 0 V dc
Logic ONE: +6 V dc
All inputs are diode buffered

*With optional hardware

Standard Input/Output Lines
10-bit address bus
16-bit input bus
16-bit output bus
Priority interrupt
External control and sense lines

I/O Teletype Unit (ASR-33 or ASR-35)
Print	10 cps
Keyboard input	10 cps
Read paper tape	10 cps
Punch paper tape	10 cps

Off-line paper tape reproduction, preparation and listing

Central Processor Options
Memory parity
Real-time clock
Memory lockout (includes sector zero relocation)

I/O Options
Additional priority interrupts
Direct multiplex control (DMC)
Direct memory access (DMA)
Parallel input or output channels
Parallel buffered I/O channels

Peripheral Options
Magnetic tape transports — 36-80 ips
Mass storage system — 100K-600K words
Line printer — 120 col, 300 lpm
Paper tape reader — 300 cps
Paper tape punch — 110 cps
Card reader — 200 cpm

OPERATION
Flexible control with simplified communication

The DDP-416 console is cable-connected to the central computer and can be positioned anywhere on the top of the cabinet to suit operator convenience. Or it can be moved to an adjacent table if preferred.

*μ*COMP DDP-416 is designed to provide high performance and simple, direct operation characteristics. Operator control specifications have been engineered for flexibility and are augmented by extensive information display. Built-in power failure protection and ease of maintenance are design features.

Control Console Functions — Standard movable console contains binary displays in octal representation, run status displays, and all operator controls. By depressing the appropriate select switch, the operator can display contents of the A register, program counter, and memory information register as well as internal counters and flip-flop status. Registers may be cleared and/or altered from the console and memory locations can be displayed or written into.

Console control functions include selection of operation mode, memory accesses, single instruction, continuous run, and a power failure interrupt inhibit switch.

In addition to the console control, the DDP-416 utilizes a teletype keyboard unit with paper tape reader and punch. Either a Model ASR-33 or ASR-35 is offered. When used in conjunction with software checkout functions, this I/O medium becomes the primary control for breakpointing programs, changing memory contents, displaying memory, and related functions. It may also be used off-line for preparation, duplication, or listing program tapes.

Power Failure Protection — Standard DDP-416 memory is protected against power failure. The memory will automatically shut down without destroying information. Also, an interrupt on power failure will occur permitting storage of register contents in memory before the memory shuts off.
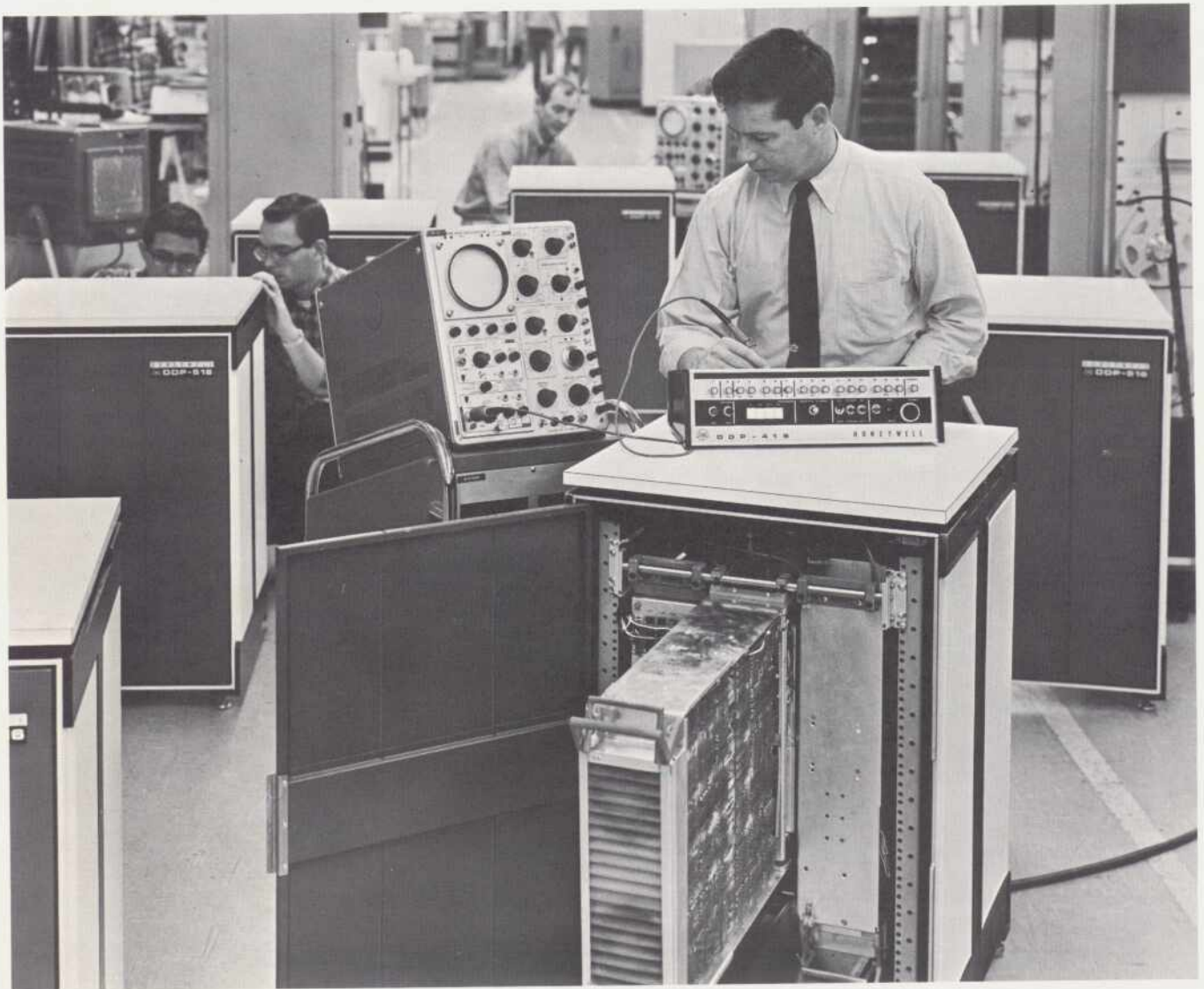
DATA REPRESENTATION AND ADDRESS MODES
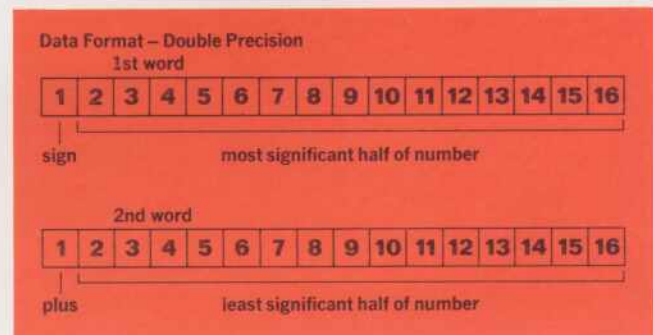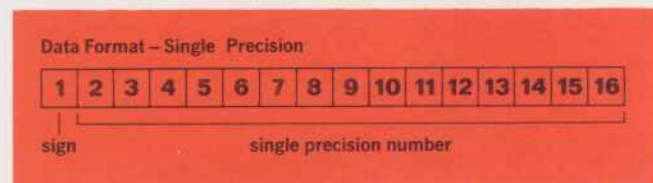**Single word instructions and large sector size for efficient operation**
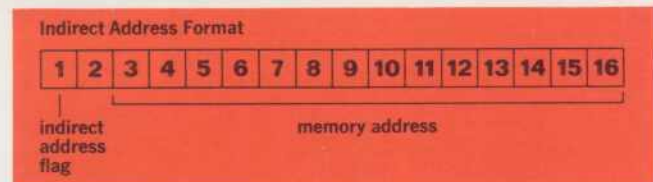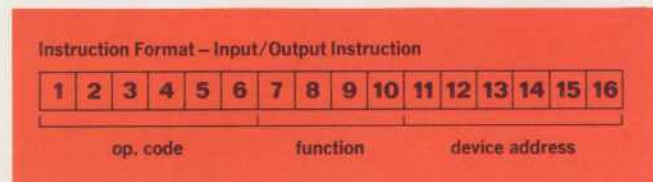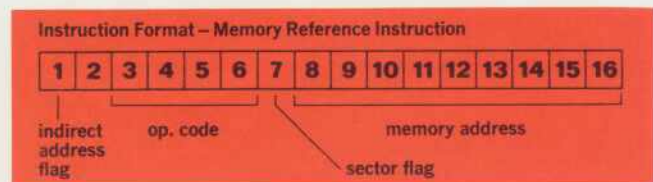
DDP-416 instructions feature a 4-bit operation code, indirect addressing capabilities, and an address field that allows 1024 words of memory to be directly addressed. Memory is organized into large 512-word sectors for ease of programming.

Sector Addressing (one word per instruction) — When the sector flag is a one, the address portion of the instruction refers to the same sector as that addressed by the program counter.

When the sector flag is a zero, the address portion of the instruction refers to a sector zero. (Note: memory lockout option includes sector zero relocation register. When sector flag is zero, instruction refers to sector whose address is in relocation register).

Indirect Addressing — When indirect addressing is required, the effective address is assumed to be in the location specified by the address portion of the instruction and the selected sector address. However, if the location specified by the address portion of the instruction and the selected sector address also calls for indirect addressing, another cycle of indirect addressing is initiated. This chaining of indirect addressing can continue indefinitely for all instructions which permit indirect addressing. Each indirect address cycle requires an additional 960 nanoseconds for instruction execution.

Fixed Point — Data is represented in two's complement form, with the sign in the most significant bit position followed by 15 magnitude bits. Single precision fixed point values thus range from $-16,384$ to $+16,384$. While this is adequate for most applications, the DDP-416 offers software double precision capabilities for users who require 30-bit accuracy.

Instruction Format – Memory Reference Instruction

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |

indirect address flag — op. code — memory address — sector flag

Instruction Format – Input/Output Instruction

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |

op. code — function — device address

Indirect Address Format

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |

indirect address flag — memory address

Data Format – Single Precision

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |

sign — single precision number

Data Format – Double Precision

1st word

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |

sign — most significant half of number

2nd word

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |

plus — least significant half of number

INSTRUCTION REPERTOIRE
Wide selection of basic arithmetic and control steps

Type	Mnemonic	Time (μsecs)	Description
Load and Store	LDA	1.92	Load A
	CRA	0.96	Clear A
	STA	1.92	Store A
Arithmetic	ADD	1.92	Add
	SUB	1.92	Subtract
	IRS	2.88	Increment, Replace and Skip
Control	SMK	1.92	Set Mask
	HLT	0.96	Halt
	NOP	0.96	No Operation
	ENB	0.96	Enable Program Interrupt
	INH	0.96	Inhibit Program Interrupt
Input-Output	OCP	1.92	Output Control Pulse
	SKS	1.92	Skip if Ready Line Set
	INA	1.92	Input to A
	OTA	1.92	Output from A
Logical	ANA	1.92	Logic AND
	ERA	1.92	Exclusive OR
Shift	LGL	$0.96 + .48n$	Logical Left Shift
	LGR	$0.96 + .48n$	Logical Right Shift
	ALR	$0.96 + .48n$	Logical Left Rotate
	ARR	$0.96 + .48n$	Logical Right Rotate
	ALS	$0.96 + .48n$	Arithmetic Left Shift
	ARS	$0.96 + .48n$	Arithmetic Right Shift
Transfer Control	JMP	0.96	Unconditional Jump
	JST	2.88	Jump and Store Location
	SKP	0.96	Unconditional Skip
	SPL	0.96	Skip if A Plus
	SMI	0.96	Skip if A Minus
	SZE	0.96	Skip if A Zero
	SNZ	0.96	Skip if A Not Zero

Optional features for expanded capability
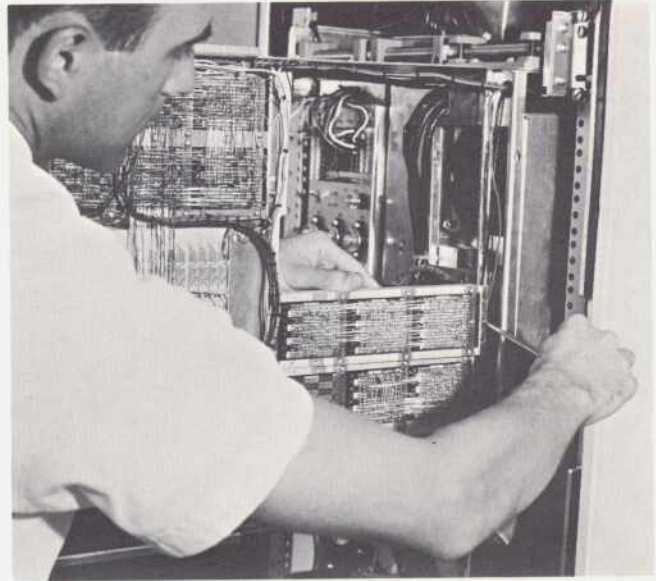
Memory Parity — Provides facilities for generating parity on all memory write cycles and checking parity on all memory read cycles. The computer's memory parity error flip-flop can be tested under program control and reset under program control. The setting of the parity error flip-flop generates an interrupt on the standard interrupt line. This interrupt can be inhibited under program control by resetting the interrupt mask. Instructions:

RMP 0.96 μsec Reset memory parity indicator
SPS 0.96 μsec Skip on memory parity error
SPN 0.96 μsec Skip on no memory parity error

Memory Lockout — Facilitates the time-shared execution of undebugged programs concurrently with on-line operation. To this end, the memory sectors containing the on-line program and its data, etc., are protected from accidental alteration.

Peripheral equipment is similarly protected to maximize system integrity.

In the restricted mode of operation, no protected location can be altered, and the operations OCP, SKS, OTA, SMK, INA, HLT, and INH are considered illegal. No instruction is permitted more than eight levels of indirect addressing in this mode. Any instruction attempting to violate these restrictions is aborted and causes an interrupt.

Normal operation is free of all restrictions; the program can execute any instruction in the repertoire. Selection of those memory sectors which are to be protected is controlled by a lockout mask register. It is a 32-bit register, each bit of which is associated with one 512-word memory sector, and contains a zero if the corresponding sector is protected. The setting is accomplished by SMK instructions. In addition, sector zero may be relocated for those programs not having access to the true sector zero. The relocated sector zero is that sector whose address is in the 6-bit relocation register.

Instructions provided with the memory lockout option include:

ERM 0.96 μsec Enter restricted mode
SMK 1.92 μsec Set relocation register
SMK 1.92 μsec Set lockout mask

Once entered, operation continues in the restricted mode until an interrupt, whether caused by a protection violation or not, occurs.

Real-Time Clock — Permits the computer to keep track of real time by means of a memory location which is incremented by one every 16.67 milliseconds. This location is usually preset by program to a minus value; when it reaches zero, an interrupt occurs.

The basic I/O system of the DDP-416 consists of an input/output bus used to transfer full words in and out of the computer. In addition it contains lines which provide timing signals and commands to peripheral devices. Each peripheral device which is tied to the I/O bus has its own buffer and control logic. This feature permits a high degree of flexibility in using multiple devices concurrently and in handling multiple devices through priority interrupt. Devices are addressed by means of the six least significant bits in an I/O instruction. These, plus four function bits, are transmitted via the 10 ADB (address bus) lines to the device where they are decoded.

Priority Interrupt — The standard interrupt system consists of a single interrupt line to which multiple interrupt sources can be connected. When an interrupt occurs the program counter is stored and control is transferred to a standard location. A software routine then sorts out the source of the interrupt and transfers to the correct subroutine. Interrupt sources can be enabled and inhibited individually under program control. Thus the system permits multiple priority interrupt levels with the stacking of interrupts upon interrupts. Assignment of the priority level of a particular source is also under program control.

I/O Modes — There are four basic modes in which data can be transferred back and forth between peripheral devices of the DDP-416.

    a. single word transfer
    b. single word transfer with interrupt
    c. direct multiplexed control (DMC)
    d. direct memory access (DMA)

Single Word Transfer Mode — The basic input/output mode of the standard computer is single word transfers under program control. In this mode, words can be read from external devices into the accumulator utilizing INA instructions, and full words can be transferred from the accumulator to the output device using OTA instructions. During input in this mode, the programmer has the option of clearing or not clearing the accumulator before each input (INA) instruction. This allows input characters to be packed into words as part of a basic input routine. In order to make the DDP-416 extremely flexible in real-time applications, the ability to test and skip on the ready status of an I/O device has been included in the basic input and output instructions. Thus the computer is not required to hold off, waiting for a ready signal. Using the single word transfer mode, blocks of input or output data may be transferred to/from memory at word rates up to 87 kc.

Single Word Data Transfer with Interrupt Mode — The interrupt system can also be utilized with the basic input/output commands to provide a powerful input/output mode for real-time processing. In this mode frequent testing of a device for readiness is eliminated. The device ready signal causes a program interrupt. The I/O functions are then performed whereupon the program continues in its normal fashion.

Additional priority interrupt lines, up to a total of 48, may be added to a DDP-416 system.

Direct Multiplexed Control (DMC) — A direct multiplexed control mode is available which permits data transfer between peripheral devices and the memory concurrent with computation. In this mode the starting location to which the block of information

is to be transferred and the final location at which the block transfer is to be terminated are set up under program control. The data transfer is then initiated by the program. Once this has been done, transfers occur independently of program control until the specified block of memory has been filled.

Since the starting and final addresses of the block of memory are stored in standard locations in memory, this is an extremely economical mode of I/O. Up to 16 devices can be connected to the DMC system simultaneously, independently transferring data between each device and a specified block in memory. Because this mode requires only 3.84 microseconds of computer time for each word transfer, a maximum word rate of 260 kc can be obtained if computation is effectively halted. For slower word rates, any time not needed by the DMC is used by the computer for computation. End of range interrupt (maskable) is a standard feature for each DMC sub-channel. An added option is DMC automatic switching, whereby end of range causes alternate blocks of memory to be used.

Direct Memory Access (DMA) — This channel provides an alternate path to memory via the L register by means of which I/O transfers may be processed on a cycle stealing basis. Up to four sub-channels, each with its own address and range registers, may be multiplexed into the DMA channel. In the time-shared mode, DMA interrupts processing for 1.2 μsecs per word. Maximum response time from data request until transfer complete is 1.92 μsecs on input, 2.64 on output. In the block transfer mode, with program processing suspended, DMA I/O rates exceed one million 16-bit words per second.

PROGRAMMING SOFTWARE
Comprehensive package is designed to meet extensive application requirements
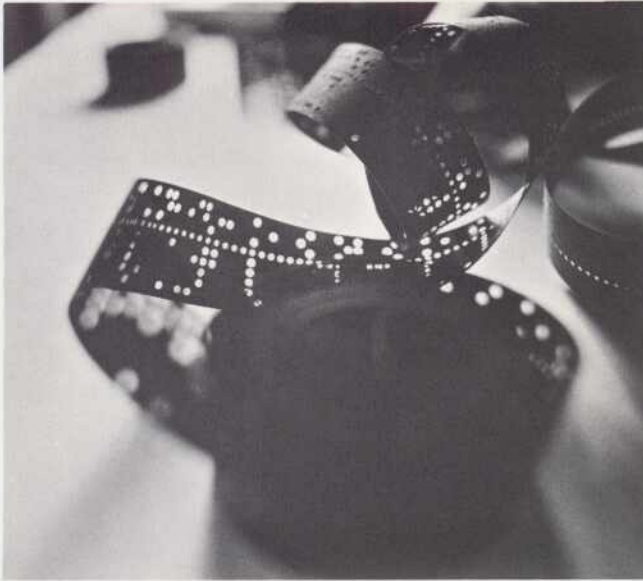
Assembly Program (DAP-16) — DAP-16 is a symbolic language assembly program. The purpose of DAP-16 is to translate from a symbolic language convenient to the programmer to binary code intelligent to the DDP-416. Translation is optionally made in a two-pass or one-pass process and is generally on a one-for-one basis, that is, for each source statement written by the programmer, one machine instruction is generated by DAP-16.

DAP-16 produces either relocatable or absolute object code, and the source language includes the capability of using symbolic addressing mnemonic machine codes, and compound address expressions. In addition, DAP-16 provides octal, decimal and ASCII literals plus a wide variety of pseudo-operations which serve to control the assembly process, define data, allocate core memory or generate linkage to subroutines.

An important feature of DAP-16 is the generation of an extended object code. The extended object code in conjunction with the DESECTORIZING loader, permits the programmer to address the DDP-416 as if the entire memory were directly addressable rather than concerning himself with sector address — and the indirect address linkage necessary to cross from sector to sector.

Input/Output Selector (IOS) — This program is used in conjunction with major programs supplied with the DDP-416 to establish the input/output communication link with the input/output equipment. Users with varying complements of peripheral equipment are readily accommodated by the modular design of IOS.

DESECTORIZING Loader — A relocatable program which loads the memory with octal information in absolute or relocatable format. This program is capable of loading the main program and subroutines called by it or called by other subroutines, and completes the transfer vector linkage between the main program and external subroutines. Also included is the capability to generate special indirect address links in sector zero based on addressing information generated by the assembly program or compiler.

Subroutine Library — The standard software package includes an extensive assortment of subroutines to aid the programmer in performing mathematical operations and functions, conversion, and input-output operations.

Mathematical routines, available for single precision, fixed point calculations, include:

multiply
divide
sine
cosine
arctangent
square root
log (base e)
log (base 2)
log (base 10)
exponential (base e)
exponential (base 2)
exponential (base 10)

and routines for the double precision math operations add, subtract, multiply and divide.

DEBUG Program — A compact relocatable program capable of:

    a. Inserting breakpoint halts

    b. Searching memory for selected instructions

    c. Dumping selected areas of memory

    d. Inspecting and conditionally changing locations in memory

    e. Punching corrected programs in load mode

The DEBUG program is controlled from the teletypewriter keyboard.

Input/Output Library — Made up of a set of subroutines for each I/O device, offered with the DDP-416. Each I/O routine permits the user to specify the data format most convenient for his application. Any necessary code conversion is handled by the I/O routine. Complete error checking and, where possible, recovery procedures are included.

Vertification and Test Programs — An extensive package of verification and test programs is provided with the DDP-416, which includes routines for verifying the operation of the control unit, arithmetic unit, core memory, and the available input/output devices. These routines generate indicative information reflecting the operational status of the equipment being verified.

INPUT/OUTPUT LIBRARY	ASCII	Binary
ASR-33	•	•
ASR-35	•	•
Paper Tape Reader	•	•
Paper Tape Punch	•	•
Card Reader	•	•
Line Printer	•	•
Magnetic Tape	•*	•
Disc File	•	•

*Includes conversion to and from IBM 729 series tape code.

DELIVERY

Immediate Delivery Reservation holds a machine while you evaluate its capabilities

If delivery is a serious factor on your computer evaluation check list, you may want to reserve a DDP-416 in advance. Simply write us on your letterhead, indicating the standard model numbers from the summary list below.

We'll confirm an approximate delivery date by return mail, and hold for 15 days while you make your decision.

Model Number	Description
416-01	DDP-416 general purpose digital computer with 4,096 words of core memory.
416-02	DDP-416 general purpose digital computer with 8,192 words of core memory.
416-03	DDP-416 general purpose digital computer with 12,288 words of core memory.
416-04	DDP-416 general purpose digital computer with 16,384 words of core memory.
416-07-1	Parity for 4K memory module.
416-07-2	Parity for 8K memory module.
416-08	Memory lockout system for 1st 8K of memory.
416-08-1	Memory lockout system for each additional 8K.
416-12	Real time clock.
416-20	Direct multiplex control unit. (DMC)
416-21	Direct memory access control unit (DMA) and one channel.
416-21-1	Additional DMA channel.
416-25	Group of 4 priority interrupt lines.
416-25-1	Additional groups of 4 priority interrupt lines.
416-26	Memory counter modification for group of 4 priority interrupt lines.
416-32	Parallel input channel.
416-33	Parallel output channel.
416-34	Buffered parallel I/O channel.
416-4100	Magnetic tape control unit, controls up to 4 transports of similar speed and density.
416-4130	36 ips Magnetic tape transport, 200/556 bpi.
416-4131	36 ips Magnetic tape transport, 200/800 bpi.
416-4132	36 ips Magnetic tape transport, 556/800 bpi.
416-4140	80 ips Magnetic tape transport, 200/556 bpi.
416-4141	80 ips Magnetic tape transport, 200/800 bpi.
416-4142	80 ips Magnetic tape transport, 556/800 bpi.
416-50	Paper tape reader, 300 cps.
416-52	Paper tape punch, 110 cps.
416-53	ASR-33 Teletype unit.
416-55	ASR-35 Teletype unit.
416-61	Card reader, 200 cpm.
416-7050	Line printer, 120 columns, 300 lines per minute.

FIELD OFFICES

Alabama
2003 Byrd Spring Rd. SW, Suite 106
Huntsville, Alabama 35802
(205) 881-2711

California
9171 Wilshire Boulevard
CEIR Building, Suite 610
Beverly Hills, Calif. 90210
(213) 278-1901

1041 DiGiulio Road
Santa Clara, Calif. 95050
(408) 241-5650

Connecticut
125 La Salle Road, Room 207
West Hartford, Connecticut 06107
(203) 523-4037

Florida
P.O. Box 5401
3986 Boulevard Center Drive
Jacksonville, Florida 32207
(904) 359-5253

1010 Executive Center Dr. - Suite 115
Orlando, Florida 32803
(305) 841-1570

Georgia
500 Plasters Avenue NE
Atlanta, Georgia 30324
(404) 875-9561

Illinois
3158 Des Plaines Avenue
Des Plaines, Illinois 60018
(312) 824-5186

Maryland
8121 Georgia Avenue
World Building, Room 700
Silver Spring, Maryland 20910
(301) 587-1712

Massachusetts
275 Wyman Street
Waltham, Mass. 02154
(617) 893-2610

Michigan
20441 James Couzens Highway
Detroit, Michigan 48235
(313) 836-7170

Missouri
2146 Hampton Avenue
St. Louis, Missouri 63139
(314) 647-6100

New Mexico
1030 San Pedro NE
Albuquerque, New Mexico 87110
(505) 268-6714

New York
104-70 Queens Boulevard
Forest Hills, New York 11375
(212) 275-6200

3001 James Street
Syracuse, New York 13206
(315) 463-4534

Ohio
1001 E. 55th Street
Cleveland, Ohio 44103
(216) 881-0300

401 Astor Avenue
Dayton, Ohio 45449
(513) 299-8771

Pennsylvania
8367 Bristol Pike
Levittown, Pa. 19054
(215) 943-2210

Bee St. at Greentree Rd.
Pittsburgh, Pa. 15220
(412) 922-4422

Texas
P.O. Box 64776
6000 No. Central Expressway
Dallas, Texas 75206
(214) 363-5441

P.O. Box 66667
3322 Richmond Avenue
Houston, Texas 77006
(713) 529-3163

Washington
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