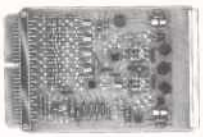
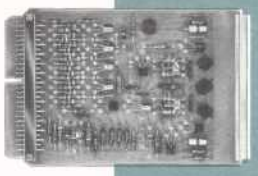
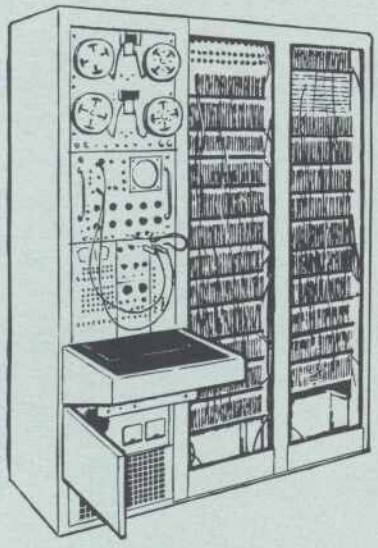
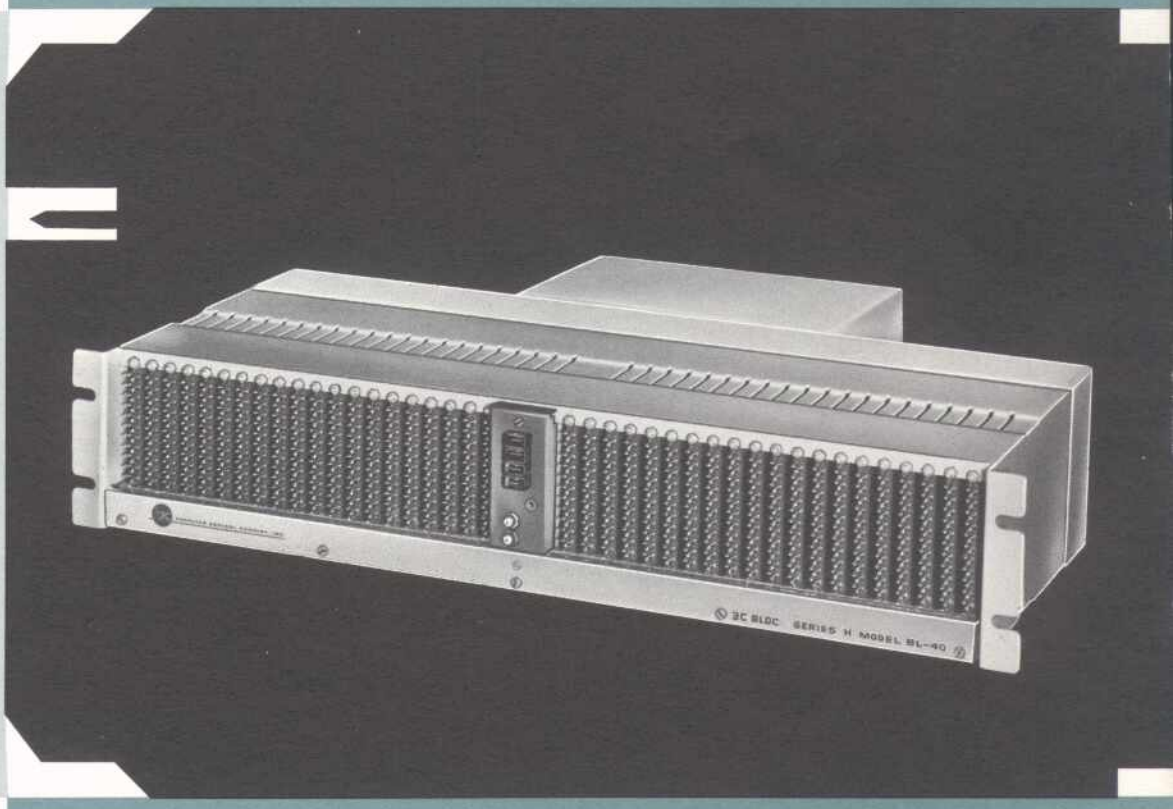
catalog H-1





16 MEGACYCLE SERIES H PACS





A comprehensive series of *10 and 16 megacycle* digital modules.

COMPUTER CONTROL COMPANY, INC.

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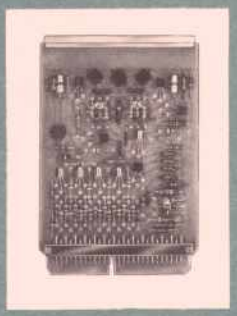


BECAUSE . . . . . . *Computer Control Company's* new 3C PACs *Series H* represent a significant advance in the current state of the art of *digital modules*, we are deviating from the type of presentation usually found in catalogs or brochures of this type.

In order to provide the reader with a maximum of pertinent and specific information devoid of promotional bias, we are substituting, instead, *a reprint of an important technical paper* which was presented recently at a major symposium on computer development.

Generalized promotional claims, therefore, are omitted in favor of this straightforward presentation. We have, however, italicized occasional major features of the H-PAC family (for emphasis) where they are mentioned, or otherwise discussed, therein.

We are pleased to supply you with our new information in this manner – the reprint, in its entirety, now follows on the opposite page:

A SYNCHRONOUS LOGIC TECHNIQUE FOR SIXTEEN MEGACYCLE CLOCK RATES

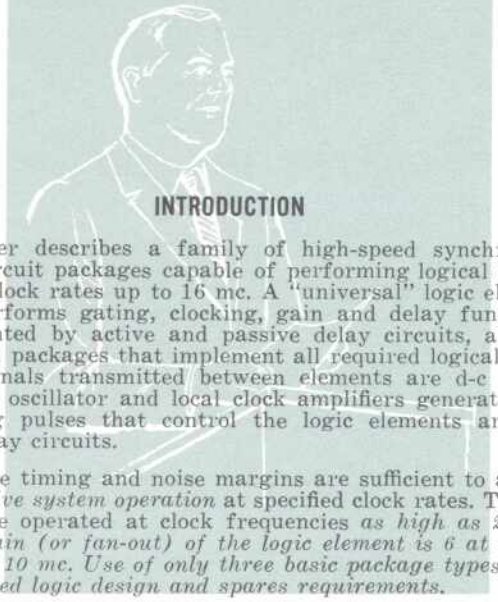
(A reprint of a technical paper presented at the 1960 Wescon Conference in Los Angeles)

By

T. P. BOTHWELL, J. L. DeCLUE,
H. H. HILL, AND J. R. LONGLAND

of

COMPUTER CONTROL COMPANY, INC.
FRAMINGHAM, MASSACHUSETTS



INTRODUCTION

This paper describes a family of high-speed synchronous digital circuit packages capable of performing logical operations at clock rates up to 16 mc. A "universal" logic element which performs gating, clocking, gain and delay functions, supplemented by active and passive delay circuits, are the functional packages that implement all required logical functions. Signals transmitted between elements are d-c levels. A master oscillator and local clock amplifiers generate synchronizing pulses that control the logic elements and the active delay circuits.

Worst-case timing and noise margins are sufficient to assure *conservative system operation* at specified clock rates. Typical units have operated at clock frequencies *as high as 25 mc. Logical gain (or fan-out) of the logic element is 6 at 16 mc and 10 at 10 mc. Use of only three basic package types leads to simplified logic design and spares requirements.*

This paper will cover principles of operation, characteristics, packaging and performance of these modules and consider some of the problems which were encountered.

SIGNAL REPRESENTATION

The maximum clock rate in most logical systems is governed by the performance limits of the individual logic elements, and the interconnection problems. At multimegacycle clock frequencies, signal inter-package transit times can represent significant delays. Considerable delay uncertainties arise from variations in transition time of circuit elements operated near their upper bandwidth limits.

Reclocking the information in each logic element *cancels out these uncertainties.* This does not, of course, increase maximum operating speed, but does clearly define timing, and therefore greatly simplifies application and debugging.

Historically, synchronous or dynamic systems have used pulse signals. However, pulse signals require that the circuit elements be capable of two transitions for each bit of information; one rise and one fall. D.C. level signals, classically used for static logic, require only a single transition per bit of information. Therefore, when a fixed time interval is available for signal transitions, D.C. level signal representation demands less stringent control of signal rise and fall time. With active circuit components whose upper frequency of operation is being approached, d.c. level signal representation permits a higher clock frequency than would pulse representation.

The marriage of static logic signals to dynamic logic results in a high operating frequency with maximum freedom from timing problems. This approach was selected for the package family described, thus combining the advantages of the logical design simplicity of dynamic techniques with the bandwidth and output signal advantages of static logic.

The logic which results is functionally equivalent to the familiar SEAC and 3C T-PAC logic, but differs in mechanization to allow optimum use of the upper frequency limit of the amplifying devices.

All the fundamental logical structures can be implemented with three package types:

1. *Logic Element:* This is the only logical package required; providing AND/OR gating, unit delay, power gain, and complementary outputs.
2. *Passive Delay:* Unit delay lines, 62.5 or 100 nsec.
3. *Active Delay:* A clocked unit delay with power gain and complementary outputs.

THE UNIVERSAL LOGIC ELEMENT

Figure 1 shows an "equivalent logic" diagram of the logical element package. Its output stage contains a static flip-flop which may change state only after a clock time as determined by the input signals. Only the d-c output levels of the flip-flop are transmitted between logic elements.

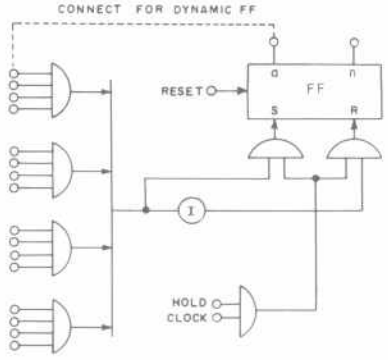


Figure 1 Logical Element

The input logic structure consists of four 4-input AND circuits followed by a 4-input buffer (OR circuit). The complement of this function is generated by inversion. The two complementary functions are gated with the clock, and applied to the flip-flop as a "set" or "reset" signal. Thus, if the logical input conditions are fulfilled, the clock pulse will "set" the flip-flop; and if not, the clock pulse will "reset" the flip-flop. The flip-flop, of course, responds only to signals that will change its state.

Three variations on this basic operation are provided for. First, two of the four input gates can be wired together to form one 8-input AND gate. Second, the clock signal may be inhibited, preserving the flip-flop contents statically. Finally, a clear input is provided to allow simultaneous resetting of all registers in a system when initial power is applied.

Circuit Operation

Figure 2 illustrates the circuit block diagram. The flip-flop is "set" or "reset" by a clocked current pulse steered through the gate transistors. The steering circuit performs two functions; buffering the input gates, and inversion. Each successive clock pulse, unless inhibited in the clock inhibit gate, produces a trigger pulse. The input logic determines whether the flip-flop will receive the trigger pulse on the set side or the reset side.

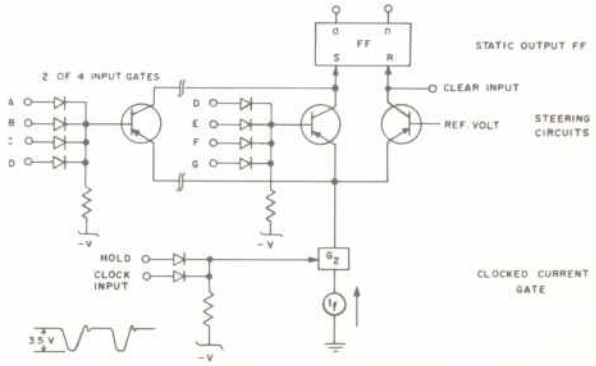


Figure 2 Simplified Schematic Diagram of Logic Element

To assure minimum delay and maximum timing tolerances, only the output stages of the flip-flop use saturating circuits. These serve as inverters and short-circuit protected emitter-followers. All other transistors operate in a non-saturated common-base mode as logic gates and as a clock pulse amplifier.

The logical structure consists of diode AND gates and a transistor buffer. The output of this four transistor buffer is applied to the "set" input of the flip-flop. The "reset" gate transistor is coupled to the input logic through a common emitter connection to the clocked current source. When none of the buffer transistors conduct, the current pulse is "steered" through the reset-gate transistor into the reset input of the flip-flop.

This gating structure has several advantages in a high speed system. The combination of diode gating and current steering provides multi-input, multi-level logic at reasonable cost. The gates receive their base conditioning voltages between clock pulses when no emitter current is flowing and only minimal input power is required to overcome stray and junction capacities in advance of the next clock pulse. The gate transistors are operated essentially grounded base, thus introducing minimum delay to the clock pulse applied at the emitter.

Input noise margins are greater than those usually exhibited by conventional inverting gates. The transfer characteristic shown in Figure 3 illustrates this effect. A definite hysteresis is produced because of unconditional clocking. That is, in normal operation, a trigger pulse is generated at every clock time and steered into the proper side of the flip-flop by the input gating structure. Thus, even if input levels were degraded or delayed to a point where half the trigger pulse is steered into either side, the flip-flop will not change state. When both sides receive approximately equal trigger energy, the flip-flop tends to remain in its present state because of its d-c regenative feedback. *The inputs must exceed the 50% steering level to cause the flip-flop to switch.* This characteristic provides generous noise margins at the inputs. To cause an error, the input must exceed the 50% steering level for the major duration of the clocking period.

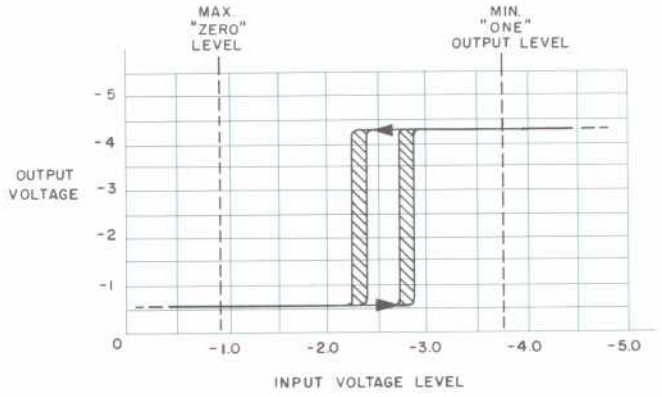


Figure 3 Typical Transfer Characteristic of Logic Element

Timing

The limits of practical operating speed, or clock rate, are determined by four timing factors:

1. Circuit transition and delay times,
2. Clock pulse position uncertainties,
3. Signal transmission delays,
4. Clock width, if pulse splitting is to be avoided.

For the family of circuits under consideration, the minimum clock period is 62.5 nsec. This time is apportioned as follows:

1. Circuit delay plus rise or fall time: 25 nsec, maximum
2. Clock pulse position tolerance: ±2.5 nsec
3. Transmission: 12 nsec. This allows for approximately 8 feet of interconnecting open wire lead.
4. Clock pulse width: 20 nsec, maximum

Figure 4 illustrates the limiting widths of clock pulses and clock timing, and relates these to allowable signal transition times.

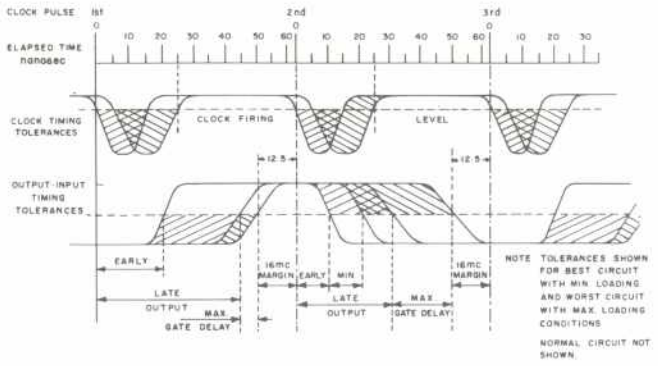


Figure 4 Signal Timing Chart at 16 mc

At lower clock rates, greater circuit and transmission delays can be tolerated, allowing heavier loading and longer leads. The loading rules permit driving six loads from each flip-flop output at 16 mc and 10 loads per output at 10 mc. Figure 5 shows typical signals at 16 mc.

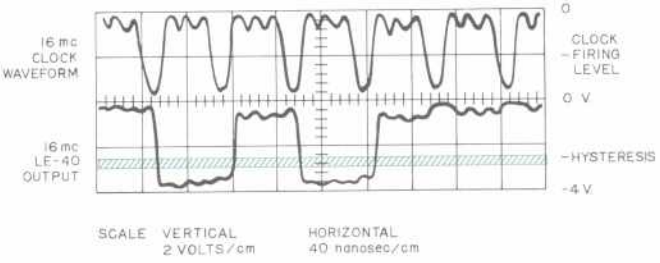


Figure 5 Typical Signals at 16 mc

Clock Pulse "Splitting"

Pulse splitting occurs when an input signal transition coincides with a clock pulse so as to steer part of the clock pulse through each of the set and reset gates. This could result from a wide or "late" clock pulse, or an "early" signal input. At the highest operating rate, the clock pluse duration is 20% to 30% of its period, and unless carefully considered in the design, pulse splitting could become a serious problem. The flip-flop could be prematurely triggered by the logic level intended for the next clock period, or could fail to respond to a signal from the previous clock period. Either case would generate an error.

The logic element circuit incorporates a circuit technique *which guarantees proper operation regardless of input signal configurations yet does not limit the maximum operating rate.* This is accomplished by effectively delaying the gating signal at the input of the logic element, so that the output can be allowed to change simultaneously with the clock pulse. Substantial margins are built into this circuit, assuring operation for the widest possible clock pulse.

PASSIVE DELAY ELEMENTS

The passive delay line is the second building block in this circuit family. A delay line can serve as a reliable shift register or storage element in a dynamic system. Passive delay lines offer a simple and low-cost approach to these functions.

The delay lines employed in this package family are m-derived, lumped parameter lines of length equal to one clock pulse period. The delay lines are quite small; six fit easily on a standard 3¼ inch by 4½ inch package. Terminating resistors are provided on all packages for wiring convenience, but the most desirable location for the termination is on the package of signal origin. This removes current flowing in the termination from system grounds.

A delay-to-rise-time ratio of 6 is adequate at 10 mc, and is obtained from an 8-section line. At 16 mc, an 8-section line provides rise times of approximately 12 nsec and improved precision of delay. The delay accuracy of individual lines is better than 2%. Uncertainties resulting from variations in the length of cascaded lines and from degradation of signal rise times limit the maximum passive delay line length to 2 units at 16 mc. At 10 mc cumulative uncertainties of 3 delay units can be tolerated.

At 16 mc, a total of 5 loads can be driven from a 2-period delay, two at the tap and 3 at the termination. At 10 mc, a total of 7 loads can be driven from the line, whatever its length. The distribution of the loads must be such that not more than 2 loads appear at any tap, nor more than 3 at the termination.

The effect of loading on a delay line is to introduce noise transients, or reflection, which have the effect of a mismatch on a properly terminated, uniform line. These reflections are re-reflected at the source, whose very low impedance appears as a short-circuit termination. The cumulative effect of these reflections is to reduce circuit noise margins. Delay line loading limitations are based on consideration of this problem so as to insure conservative, reliable operation.

ACTIVE DELAY ELEMENTS

The third building block of the family is an active delay element. This is a logic element circuit without input logic. Output signals and loading characteristics are essentially identical to those of the logic element, but only a simple two-input gate is provided at the input. In addition, clear and clock inhibit inputs are provided.

For 16 mc operation, long delay circuits require an active delay or a logic element following each two passive delay units.

CLOCK GENERATION AND DISTRIBUTION

The subject of clocking is divisible into three topics: (1) a master oscillator; (2) a local or slave clock; (3) transmission of signals from master oscillator to slave clock; and signal transmission from slave clock to logic elements.

The master oscillator is the basic timing generator. It provides sufficient power for controlling 12 local clocks. The local clock is an intermediate amplifier which receives signals from the master oscillator, performs necessary shaping and amplification, and distributes clock pulses to logic elements.

The Master Clock

The master clock consists of a Colpitts type oscillator and an amplifier. The circuit is amplitude-stabilized to assure linear operation and a clean sinusoidal output over a wide range of transistor characteristics.

The operating frequency can be preset to any frequency between 8 and 16 megacycles by selection of appropriate oscillator components, and can be stabilized by either an internal quartz crystal or by an external synchronizing source. The output amplifier delivers a sinusoidal signal of 10 volts peak-to-peak into a 50 ohm load.

Master Clock Distribution

The master clock signal is transmitted to the various local clocks through a single terminated coaxial cable. A "T" connector ties each local clock to this single cable. The master clock always sees approximately 50 ohms, since the termination is adjusted to compensate for the number of local clock loads.

There will be a considerable phase shift between the first and last slave clock load on a single coaxial cable, due to cable delay, reflections, etc. To correct for this and for non-uniformity of local clock amplifier delays, each slave clock has an adjustable delay. These delays are set to assure simultaneous clock signals throughout the system to within ± 2 nsec.

The Local Clock

The local clock consists of a pulse-forming circuit, a high-gain squaring amplifier, and a complementary output driver. The input signal from the master oscillator is delayed a fraction of a period and gated with itself to produce a narrow pulse which is applied to the squaring circuit. Driving capability for 40 logic elements is required for a full 19 inch card frame (bloc). To accomplish this, four pulse amplifiers are driven from each pulse forming circuit, with each pulse amplifier driving ten logic elements.

SIGNAL TRANSMISSION

The nominal delay per foot of open-wire lines with standard PVC insulation is 1.5 nsec. Teflon insulation reduces this figure slightly. The maximum length of a signal wire is, therefore, limited by timing tolerances. However, where wire lengths do not exceed 3 feet, transmission delays can be neglected in logic design, since these are corrected by re-clocking. In cases where passive delay units are not involved, *lead lengths up to 8 feet are allowable.*

All open wire signal leads should be considered as transmission lines and should be terminated in a resistor approximating their characteristic impedance whenever lengths become sufficient to cause reflection problems. The characteristic impedance of open wire leads in backboard wiring is between 200 and 500 ohms. Normally, all loaded outputs are terminated at the driving package.

Serial interconnection of loads from a single output is recommended to minimize lead length and to facilitate termination. Serial wiring from load to load requires only one termination, thus the source sees the effective impedance of a single transmission line.

PACKAGING, WIRING, AND HARDWARE

This part of the development program sought to achieve a packaging technique compatible with the requirements of a 16 megacycle digital system. *A major objective was to keep the construction simple and sufficiently conventional to allow wiring and operation by people familiar with present-day techniques.* The equipment is miniaturized but not micro-miniaturized. *All components are standard commercially available hardware* and the packages are removable modules which can be repaired by competent technicians.

Miniaturization allows minimum lead lengths while providing for the use of the maximum number of packages within the limits of allowable signal transmission distances. At maximum packaging density, using relay rack mounting, a three foot lead will reach from any single package to approximately 600 other package positions.

The circuits are packaged on conventional printed circuit cards approximately 3¼ inches by 4½ inches overall. Forty such packages, together with their local clock drivers can be housed in a rack mounting bloc, approximately 3½ inches by 5 inches by 19 inches, excluding a cooling fan. Power, ground and local clock signals are distributed from the center of the bloc.

Backboard interconnections are made with open wiring. Signal crosstalk is minimized by the non-return-to-zero logic scheme; that is, *signal transitions, the source of crosstalk, must occur in the interclock pulse period.* Clock signals are carefully routed away from signal wiring to minimize coupling between clock and signals.

Each logical element package consumes approximately 1.2 watts; each active delay circuit, approximately 2.1 watts. Since a Bloc has space for 40 packages and a local clock driver, substantial power can be dissipated in a small volume. All packages are rated for operation at 50°C ambient, but when all package slots in a bloc are used, forced air cooling is required to prevent an excessive temperature rise. A simple forced air cooling device is provided with each bloc, and provides approximately 25 cubic feet of air per minute through the bloc. This air flow is sufficient to limit the maximum hot-spot temperature within a fully loaded bloc to approximately 5°C above ambient. For drawer mounting, a pressurized relay rack is necessary and cooling air should be forced from the bottom to the top of the rack. Again 25 cubic feet of air per minute per bloc is recommended. Refrigeration or heat sinking is not required.

CONCLUSION

The packages previously described are designed to be versatile, reliable system building blocks, and will be offered commercially in the near future.

Two additional packages are required to make this package family complete. These are: (1) a synchronizing element, and (2) a large scale 10 and 16 mc storage element.*

The synchronizing unit requires differentiating and shaping circuits to condition the unsynchronized signal and one or two logic elements to produce a single synchronized signal. A single package to perform this function is included.

A large scale storage element is under development, in the form of a sonic delay line. Storage of as many as 1000 bits at 16 mc appears feasible.

The authors wish to acknowledge the contributions of Franklin R. Dean and Robert D. Forsberg of Computer Control Company, Inc. to the development program and to this paper.

*SG-40/46 and SM-40 packages are now available.

MODEL

LE-40

Logical Element

The LE-40 is the basic logical element of the H-PAC family. The logical structure consists of four 4-input AND gates which buffer into the steering circuit. This circuit couples to an output stage equivalent to a static flip-flop circuit. Two 4-input gates may be joined internally to form an 8-input gate. The LE-40 may be operated as a static flip-flop or as a dynamic logic element at any clock rate UP TO SIXTEEN MEGACYCLES. Standard clock frequencies are 10mc and 16mc.

The RESET input clears the output stage to ZERO. It is intended for manual or other non-logical resetting of the output flip-flop. Both ASSERTION and NEGATION outputs are available. The output driving capability is 10 unit loads at 10mc and 6 unit loads at 16mc. Generally stated, each output is independently capable of sustaining 100 megacycle-load products in the 10 to 16mc range. The LE-40 is designed to operate with maximum loading simultaneously on both outputs. Change of state or signal level transition at the outputs automatically occurs between clock pulses.

The HOLD input decouples the gating structure from the output flip-flop stage during the presence of a logical ZERO at this input. The output flip-flop will remain static in its existing state during the presence of a HOLD input regardless of the signals at the gating structure inputs.

MODEL

DA-40

Active Delay Element

The DA-40 contains two independent LE-40 circuits minus the comprehensive gating structures of the LE-40. Each DA-40 circuit contains a 2 input AND gate. The input and output signals, operating margins, and load driving capabilities are identical with the LE-40. The DA-40 also contains HOLD inputs and a non-logical RESET input.

The function of the DA-40 is to provide two independent circuits in one PAC, each of which is capable of one pulse period of clock delay with logical gain equal to the LE-40.

The primary applications for a DA-40 are (1) in a tandem series of delay elements (DP-40 or DP-46) where the delayed signal must be reclocked, reshaped, and reamplified every two or three passive delay periods and (2) as a shift register at clock frequency. In H-PAC systems a long series of unit delays is implemented by using two (at 16mc) or three (at 10mc) pulse periods of passive delay line (DP-40 or DP-46) followed by an Active Delay circuit. With two Active Delay circuits per PAC in the DA-40 and six passive circuits per PAC in the DP-40/46, a serial delay line can be implemented with economy of space and equipment.

Additionally each element of the DA-40 can be utilized to perform other logical functions within the limits of its input gating structure such as shift registers, storage registers, flip-flops, etc.

The HOLD input on each DA circuit provides useful logical flexibility. The presence of a ZERO input signal inhibits the clock signal and thereby "holds" or maintains the existing

MODEL

DP-46

Unit Delay PAC

The DP-46 consists of six 62 nanosecond, 150 ohm electrical delay lines designed for 16 megacycle operation. The individual 62 nanosecond units of delay can be used independently or they may be cascaded. These delay units serve as reliable circulating registers, storage elements, etc. They provide a simple and low cost approach to the implementation of many logical functions.

The delay lines employed in the DP-46 are m-derived, lumped parameter lines of length equal to the clock pulse period at 16mc. A unit delay provides a rise time of approximately 12 nanoseconds when driven from an LE-40. Delay accuracy is better than 2%. Two unit delays of the DP-46 may be cascaded. For longer delay chains, the DA-40 or the LE-40 is used for reclocking. Two unit loads can be driven from the taps in a DP-46 and three loads can be placed at the termination. Terminating resistors to match the characteristic impedance of the DP-46 delay lines are contained within the driver PACs (D-40 or LE-40).

MODEL

DP-40

Unit Delay PAC

The DP-40 consists of six 100 nanoseconds, 100 Ohm delay lines designed for 10 megacycle operation. Three units of delay may be cascaded before an intervening Active Delay circuit is required. A total of seven loads can be driven from the cascaded elements of the DP-40. Loads should be distributed such that not more than two appear at any tap or more than three at the termination. Additional terminating resistors are contained within the DP-40 PAC to provide the necessary impedance match with the lower characteristic impedance of the DP-40. In all other respects the DP-40 and DP-46 are identical as to characteristics and usage.

MODEL

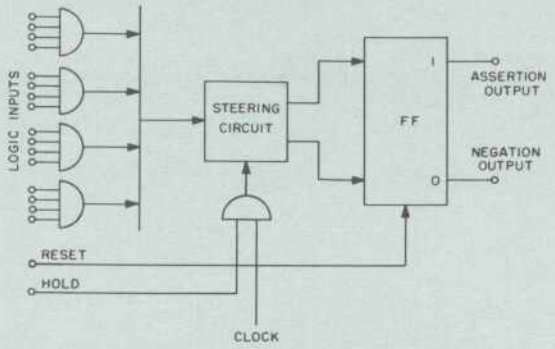
PA-40

Power Amplifier

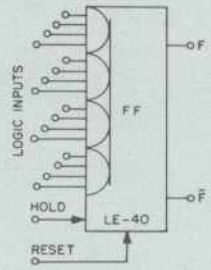
The PA-40 contains two power amplifier (PA) circuits compatible with LE-40 and DA-40 outputs. This PAC allows increased load driving capability for cases where greater fanout is required. Each input presents 3 unit H-PAC loads to the driving source; each output can drive up to 20 H-PAC loads. Thus, any LE-40 output can drive 2 PA circuits, allowing a total load driving capability of 40 loads from that output. Circuit delay is 4 nsec maximum, allowing *a net worst case* 16 mc transmission delays of 8 nsec. The PAC is not intended for use as an amplifier on DP-40/46 tap points, or as a driver for HOLD inputs.

SPECIFICATIONS

ZERO Level	−0.5 volt nominal
ONE Level	−4.0 volts nominal
Power Requirements per PAC:	
+12 volts	20 ma.
− 4 volts	33 ma.
−12 volts	70 ma.
Maximum PAC Dissipation	1.2 watts
Input Loading:	
Gate Inputs	1 unit load
HOLD Input	2 unit loads
Clock Input	1 unit clock load
RESET Input (non-logic)	40 ma. maximum
Output Drive Capability:	
Assertion }	6 unit loads @ 16mc
Negation }	10 unit loads @ 10mc
Number of circuits per PAC	One



LE-40 FUNCTIONAL DIAGRAM

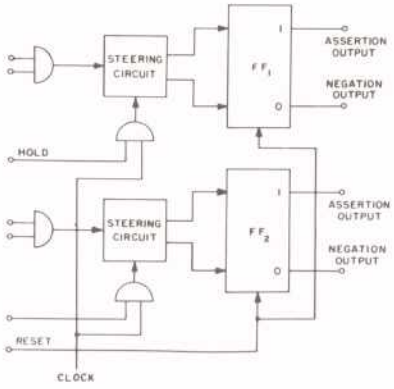


LE-40 SYMBOLIC DIAGRAM

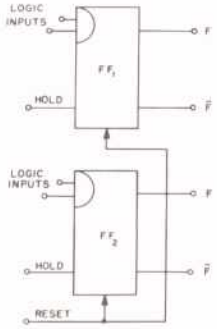
static state of the output flip-flop until the hold is removed.

SPECIFICATIONS

Number of Active Delays per PAC:	2
ZERO Level	−0.5 volt nominal
ONE Level	−4.0 volts nominal
Power Requirements per PAC:	
+12 volts	38 ma.
− 4 volts	66 ma.
−12 volts	120 ma.
Maximum PAC Dissipation	2.16 watts
Input Loading:	
Gate Inputs	1 unit load
HOLD Input	2 unit loads
Clock Input	2 unit clock loads
RESET Input (non-logic)	80 ma. maximum
Output Load Driving Capability:	
Assertion }	6 unit loads @ 16mc
Negation }	10 unit loads @ 10mc
Number of circuits per PAC	Two



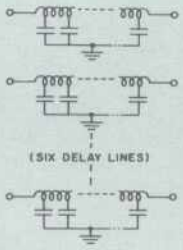
DA-40 FUNCTIONAL DIAGRAM



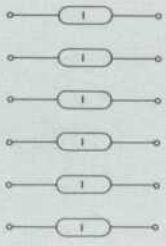
DA-40 SYMBOLIC DIAGRAM

SPECIFICATIONS

Number of Unit Delays per PAC	Six
Characteristic Impedance	150 ohms
Unit Delay	62 nanoseconds — ±2%
Delay-to-Rise-Time Ratio	Six
Type of Network	m-derived lumped constant LC
Driving Capability	5 loads total
Cascade Capability	2 units
Power Requirements	none



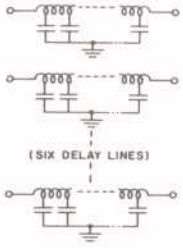
DP-46 SCHEMATIC DIAGRAM



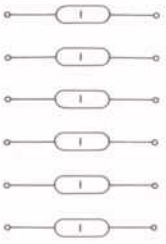
DP-46 FUNCTIONAL/SYMBOLIC DIAGRAM

SPECIFICATIONS

Number of Unit Delays per PAC	Six
Characteristic Impedance	100 ohms
Unit Delay	100 nanoseconds ±2%
Delay-to-Rise-Time Ratio	Six
Type of Network	m-derived lumped constant LC
Driving Capability	7 loads total
Cascade Capability	3 units
Power Requirements per PAC:	
+12 volts	none
− 4 volts	80 ma. maximum
−12 volts	none
Total Power dissipation	320 milliwatts



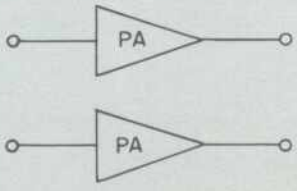
DP-40 SCHEMATIC DIAGRAM



DP-40 FUNCTIONAL/SYMBOLIC DIAGRAM

SPECIFICATIONS

ZERO Level	0.4 volts
ONE Level	4.0 volts
Power Requirements per PAC:	
+12	160 ma @ full load 20 ma @ no load
−4	
−12	160 ma @ full load 20 ma @ no load
Maximum PAC Dissipation	4 watts
Input Loading (per circuit)	3 unit loads
Clock Loading	none
Output Drive Capability	20 unit loads or 52-ohm coaxial cable
Maximum Circuit Delay	4 nsec



PA-40 FUNCTIONAL DIAGRAM

MODEL

SG-46

Synchronous Generator PAC

The purpose of the Synchronous Generator PAC is to accept a randomly timed, arbitrarily shaped input pulse, such as might be obtained from a relay, switch, paper tape reader, magnetic tape read amplifier, etc. and to convert it into one and only one properly timed and properly shaped pulse identical with the standard wave forms used in the 16mc H-PAC family. The assertion and negation outputs of the SG-46 are identical to the LE-40 with respect to amplitudes, levels, wave forms, and load driving capabilities. The input signal to the SG-46 is coupled in through any one of three pin connections on the connector. The three input terminals provide one dc coupled input and two ac coupled inputs. The choice of input terminal is dependent on the characteristics of the input signal.

The D.C. input allows the maximum input signal frequency range and independence from duty cycle considerations. Using the D.C. input, frequencies from ZERO to 7.6 megacycles may be synchronized. The D.C. input must cross the −2.5 volts level to generate an output. Duty cycle requirements are non-critical except at the higher repetition frequencies. Minimum duration of the negative going input is 65 nanoseconds.

The slowest A.C. coupled input signal which the SG-46 will recognize and convert is a negative-going waveform of 4 volts with a fall time of 2.7μs.

SPECIFICATIONS

D.C. Input		
Signal Level		0 to −10 volts maximum 0 to −4 volts minimum
input repetition frequency	D.C. to	7.6 megacycles maximum
input signal duration		65 nanoseconds minimum
input impedance		1K Ω

MODEL

SG-40

Synchronous Generator PAC

The SG-40 is identical to the SG-46 except for the duration of the output wave form. The output pulse duration of the SG-40 is 100 nanoseconds for use with the MO-40 master clock in 10mc H-PAC systems.

SPECIFICATIONS

D.C. Input		
Signal level		0 to −10 volts maximum 0 to −4 volts minimum
input repetition frequency	D.C. to	4.75 megacycles maximum
input signal duration		110 nanoseconds minimum
input impedance		1KΩ
A.C.$_1$ Input		
input signal ramp:		−36 volts per microsecond minimum
input signal amplitude:		4 volts negative going minimum
input repetition frequency:		1.2 megacycles maximum at 50% duty cycle
input impedance:		500 ohms approximately
A.C.$_2$ Input		
input signal ramp:		−1.5 volts per microsecond minimum

MODEL

MO-46

Master Oscillator

The MO-46 is a 16 megacycle crystal controlled Colpitts oscillator driving a sine wave power amplifier. The MO-46 is used in H-PAC systems as the master clock which drives all of the SC-46 slave clocks in the system. The MO-46 can drive up to 20 slave clocks. The oscillator circuit is amplitude stabilized to insure reliable linear operation and undistorted sinusoidal output over a wide range of component characteristics. The output amplifier delivers 8 volts peak-to-peak of sinusoidal signal into a 50 ohm load. Distribution to the individual local slave clocks in a multi H-BLOC system is via coaxial cable. The MO-46 occupies two connector positions in the H-BLOC and may be located in any H-BLOC in a multi-BLOC system.

NOTE: The MO-46 may be converted to external synchronization by removing the oscillator crystal and inserting an appropriate input transformer.

MODEL

MO-40

Master Oscillator

The MO-40 is the 10 megacycle version of the MO-46. It is identical to the MO-46 in all characteristics except output frequency.

SPECIFICATIONS

Output voltage:	8 volts peak-to-peak nominal
Output impedance	51 ohms
Frequency, crystal controlled	10mc ±.005%
Output DC reference level	0 volts

MODEL

SC-46

Slave Clock

The SC-46 accepts the 16 megacycle sine wave output of the MO-46 at a high impedance level and produces a negative-going H-PAC clock pulse at a low impedance level. The output signal is synchronized to the input sine wave and is adjustable in phase and width. The SC-46 contains four plug-in sub-module buffer/driver amplifiers (SCB-40) providing clock drive capability for a maximum of 48 logic elements. The SC-46 package also contains power supply bypass capacitors for the H-BLOC into which it is inserted. The SC-46 plugs into the center connector of the H-BLOC.

This connector is pre-wired to the H-BLOC low impedance clock distribution busses. These busses are transmission lines which have a nominal characteristic impedance of 20 ohms. The low impedance clock distribution system makes the clock signal amplitude and wave form essentially independent of loading changes due to insertion or removal of the H-PACs from the system.

SPECIFICATIONS

Input sine wave amplitude	6 to 10 volts peak-to-peak
Frequency	16 megacycles

MODEL

SC-40

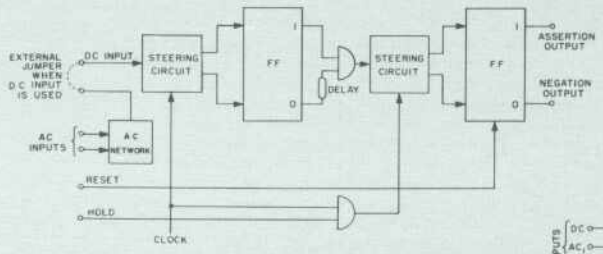
Slave Clock

The SC-40 is identical to the SC-46 in all respects except that the tuned elements of the circuit are designed to accept a 10 megacycle sine wave input from the MO-40 instead of the 16 megacycle wave form of the SC-46.

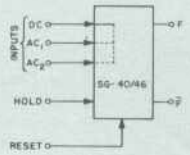
SPECIFICATIONS

Input sine wave amplitude	6 to 10 volts peak-to-peak
Frequency	10 megacycles
Output amplitude	−3.0 volts nominal
DC voltage reference level	−0.5 volts nominal
Output pulse duration (at half amplitude)	20 nanoseconds
Rise time (10% to 90%)	7 nanoseconds

A.C.$_1$ Input	
input signal ramp:	−36 volts per microsecond minimum
input signal amplitude:	4 volts negative going minimum
input repetition frequency:	1.2 megacycles maximum at 50% duty cycle
input impedance:	500 ohms approximately
A.C.$_2$ Input	
input signal ramp:	−1.5 volts per microsecond minimum
input signal amplitude:	4 volts negative going minimum
input repetition frequency:	depends upon duty cycle of negative portion of signal 80KC maximum at 50% duty cycle
input impedance:	500 ohms approximately
Power Requirements per PAC:	
+12 volts	41 ma.
− 4 volts	25 ma.
−12 volts	112 ma.
Maximum total PAC dissipation	1.9 watts
Output pulse duration	62 nanoseconds
Output Drive capability:	
Assertion	6 unit loads per output
Negation	
Number of circuits per PAC	One

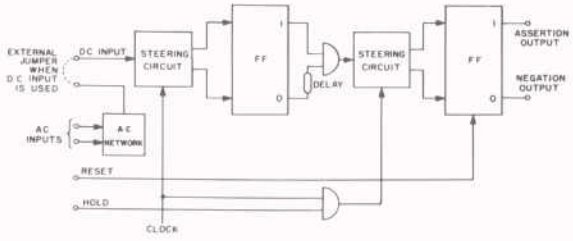


SG-46 FUNCTIONAL DIAGRAM

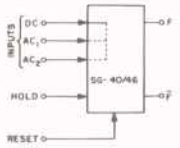


SG-46 SYMBOLIC DIAGRAM

input signal amplitude:	4 volts negative going minimum
input repetition frequency:	depends upon duty cycle of negative portion of signal 80KC maximum at 50% duty cycle
input impedance:	500 ohms approximately
Power Requirements per PAC:	
+12 volts	41 ma.
− 4 volts	25 ma.
−12 volts	112 ma.
Maximum total PAC dissipation	1.9 watts
Output pulse duration	100 nanoseconds
Output Drive Capability:	
Assertion	10 unit loads per output
Negation	
Number of circuits per PAC	One



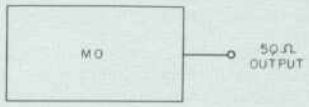
SG-40 FUNCTIONAL DIAGRAM



SG-40 SYMBOLIC DIAGRAM

SPECIFICATIONS

Output voltage:	8 volts peak-to-peak nominal
Output impedance	51 ohms
Frequency, crystal controlled	16mc ±.005%
Output DC reference level	0 volts
Output wave form	sinusoidal
Output drive capability	20 SC-46 inputs
Power Requirements per PAC:	
+12 volts	94 ma
− 4 volts	not used
−12 volts	170 ma
Maximum power dissipation	3.2 watts

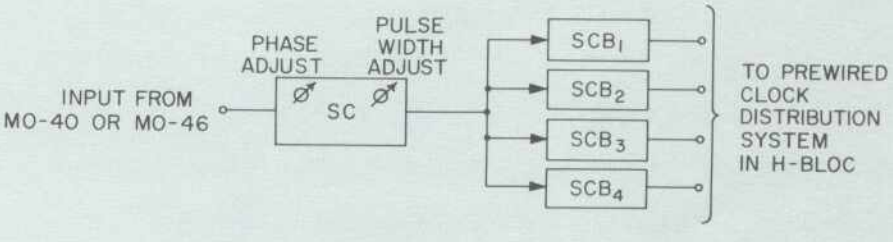


MO-46 FUNCTIONAL DIAGRAM

Output wave form	sinusoidal
Output drive capability	20 SC-40 inputs
Power requirements per PAC:	
+12 volts	94 ma
− 4 volts	not used
−12 volts	170 ma
Maximum power dissipation	3.2 watts

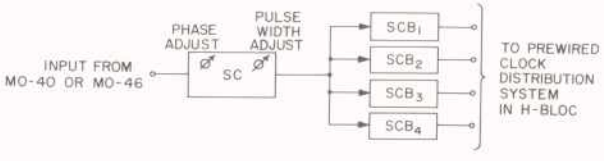
MO-40 FUNCTIONAL DIAGRAM

Output amplitude	−3.0 volts nominal
DC voltage reference level	−0.5 volts nominal
Output pulse width (at half amplitude)	20 nanoseconds nominal
Rise time — 10% to 90%	7 nanoseconds nominal
Fall time — 10% to 90%	7 nanoseconds nominal
Output drive capabilities per SC-46	48 H-PAC unit clock loads
Power requirements per PAC:	
+12 volts	100 ma. maximum
− 4 volts	50 ma. maximum
−12 volts	100 ma. maximum
Maximum total power dissipation	2.6 watts



SC-46 FUNCTIONAL DIAGRAM

Fall time (10% to 90%)	7 nanoseconds
Output drive capabilities	48 H-PAC unit clock loads
Power Requirements per PAC:	
+12 volts	100 ma. maximum
− 4 volts	50 ma. maximum
−12 volts	100 ma. maximum
Maximum total power dissipation	2.6 watts



SC-40 FUNCTIONAL DIAGRAM

MODEL

SM-40

Serial Memory PAC

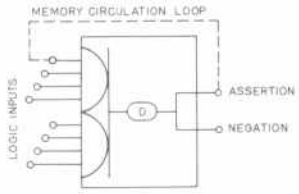
The SM-40 is a plug-in serial acoustic delay storage element with capacities ranging from 160 bits to 1600 bits at operating frequencies of 8 to 16 mc, respectively. Pulse delays of 20 μsec to 100 μsec are obtained by means of a zero temperature coefficient glass delay line which obviates the requirement for temperature control within rated limits. Longer delays and increased storage capacity can be obtained by cascading several SM-40 units directly, without the need for inter-unit drivers or temperature control. A serial memory is achieved by feeding the SM-40 output back to the input and recirculating the stored data.

The SM-40 contains all necessary input-output logic and requires only standard H-PAC clock pulses and voltage sources to provide standard H-PAC level outputs delayed from the inputs as required. The assertion and negation outputs are each capable of driving 10 unit loads at 10 mc and 6 unit loads at 16 mc. Gate inputs represent 1 unit load and the clock input represents 2 unit clock loads.

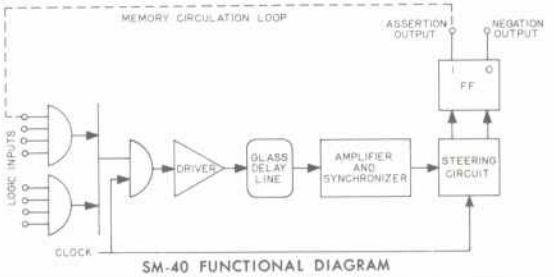
Physically, the SM-40 consists of a conventional H-PAC printed circuit card which contains input gating logic, a driver circuit, synchronizing and steering circuits, and an output flip-flop. Attached to the card, and elevated on standoffs, is a double-layer shielded enclosure which houses the glass delay line and an associated output amplifier with a fine delay adjustment of 100 nanoseconds. The entire package plugs into a single connector of the H-BLOC and occupies 4 standard card slots.

SPECIFICATIONS

Operating frequency	8 to 16 megacycles
Storage capacity	per customer specifications
Maximum storage capacity	1600 bits @ 16 mc
Delay medium	zero temperature coefficient glass
Temperature compensation	none
Ambient temperature range	0°C to 50°C
Logic Inputs	
ZERO Level	−0.5 volt nominal
ONE Level	−4.0 volts nominal
Clock Input	
Pulse Amplitude	−3 volts nominal
Pulse Width	20 nanoseconds nominal
Input Impedance	200 ohms nominal
Input Loading	
Gate Inputs	1 unit load
Clock Input	2 unit clock loads
Output Drive Capability	
Assertion |	6 unit loads @ 16 mc
Negation \	10 unit loads @ 10 mc
Power Requirements per PAC:	
+12 volts	60 ma.
− 4 volts	100 ma.
−12 volts	120 ma.
Total Power Dissipation	2.6 watts (full load)



SM-40 SYMBOLIC DIAGRAM



SM-40 FUNCTIONAL DIAGRAM

MODEL

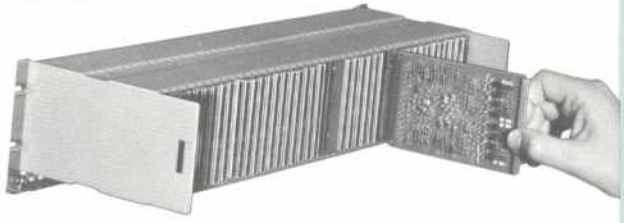
BL-40

H-BLOC

The BL-40 has provision for 40 H-PACs of any type plus an SC-40/46 Slave Clock. The Slave Clock plugs into its own connector in the center of the BLOC. A clock test point is provided as a convenience in the front center panel of the BLOC. A low impedance clock distribution system is pre-wired on each H-BLOC. Power distribution busses are also pre-wired. The pre-wired power and clock distribution systems are protected by the transverse bezel mounted along the bottom of the BLOC.

An accessory Cooling Unit (CU-40) also acts as a retainer bar for the H-PACs in the BLOC. Overall dimensions of the H-BLOC plus Cooling Unit are 3½" high by 19" wide by 12½" deep. The H-PAC connectors contained in the BLOC are designed specifically for the H-PAC Series to provide high reliability and compactness. Mating male and female connectors utilize gold-plated pin and tuning fork format. The female connector is mounted in the H-BLOC and utilizes solder terminals for inter-PAC wiring.

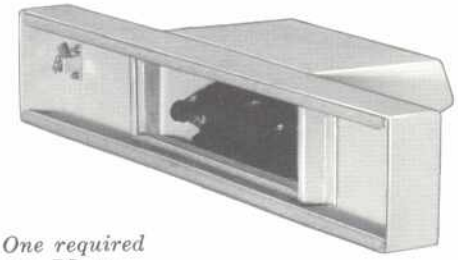
H-BLOC construction is welded steel. Finish is textured high durability vinyl enamel on a bonderized base.



MODEL

CU-40

Cooling Unit



One required per BL-40

The CU-40 is conservatively designed to provide filtered cooling air at an ambient temperature range of 0°C to 50°C for one complete H-BLOC. Air filtering is by a permanent, washable filter which is indefinitely reusable. Filter rejuvenation does not require special solvents. Air flow is provided by a motor driven fan which has adequate power capacity to move 25 CFM under the most adverse conditions. Fan operation and air flow are inaudible. The Cooling Unit mounts on the rear of the H-BLOC by means of convenient captive spring-pressured latches. A sponge rubber gasket provides air-tight coupling. Power requirement is 110 volts AC, 60 cycles at 14 watts.

MODEL

BP-40

Blank PAC

The Blank H-PAC, Model BP-40 is a standard H-PAC card with etched power and ground busses from the appropriate connector terminals around its periphery. The bulk of the card is blank for the convenient mounting of any special circuits or components as desired by means of standard component lugs and point-to-point wiring. The usable area is 7½ square inches. Drilling, lugging, and point-to-point wiring of components and circuits do not require special skills and are readily performed. It should be noted that maximum permissible component height above the surface of the BP-40 is 0.25". Exceeding this height will require that the adjoining PAC slot be left vacant. Slot spacing in the BL-40 is 0.4".

MODEL

XP-40

PAC Extender

The function of the PAC Extender is to provide unobstructed access to any PAC while it is still electrically mounted in its appropriate H-BLOC Connector. The connector terminals on the front end of the XP-40 will mount into any H-BLOC connector and the connector on the rear of the XP-40 will accept the H-PAC which it is displacing. Front and rear terminals are directly tied together electrically.

MODELS

RP-40
RP-41
RP-42

Power Supplies

The model RP rack mounted power supplies feature output regulated, line voltage stabilized, solid state circuits. Input voltage is 115 volts ±10%, 60 cycles. Three separate supply voltages are provided as required by the H-PAC circuits. These are +12 volts, −4 volts, and −12 volts. All three voltages are set screw adjustable. Overall supply voltage variations due to worst case combinations of input line voltage changes, DC load regulation, dynamic load regulation, ripple, long term drift, etc. are less than 2%. This is well within the ±10% H-PAC tolerances. Environmental operating temperature range is 10°C to 50°C. The AC line input is fused. An alarm indicator light on the front panel automatically illuminates in the event of any output voltage failure. Fast acting circuit breakers are provided in the output circuits.

SPECIFICATIONS

	Model RP-40 (5¼" x 19" x 13")		
	−12 volts	+12 volts	−4 volts
Maximum output current	@ 4 A	@ 1½ A	@ 2 A
Minimum H-BLOC capacity 1 BLOC			

	Model RP-41 (7" x 19" x 15")		
	−12 volts	+12 volts	−4 volts
Maximum output current	@ 16 A	@ 6 A	@ 8 A
Minimum H-BLOC capacity 4 BLOCs			

	Model RP-42 (14 " x 19" x 15")		
	−12 volts	+12 volts	−4 volts
Maximum output current	@ 40 A	@ 15 A	@ 20 A
Minimum H-BLOC capacity 10 BLOCS			

3C

PRICE LIST H-PAC

HIGH-SPEED, SYNCHRONOUS LOGIC, 10 AND 16 MEGACYCLE PLUG-IN DIGITAL MODULES

MODEL	DESCRIPTION	UNIT PRICE
LE-40	Logical Element (for 10 or 16 mc operation)	$ 249.00
DA-40	Active Delay (2 active delays per PAC — for 10 or 16 mc operation)	312.00
DP-46	Unit Delay PAC (6 delays per PAC — for 16 mc operation)	66.00
DP-40	Unit Delay PAC (6 delays per PAC — for 10 mc operation)	66.00
PA-40	Power Amplifier	129.00
SG-46	Synchronous Generator (for 16 mc operation)	285.00
SG-40	Synchronous Generator (for 10 mc operation)	285.00
MO-46	Master Oscillator (for 16 mc operation)	195.00
MO-40	Master Oscillator (for 10 mc operation)	195.00
SC-46	Slave Clock (for 16 mc operation)	385.00
SC-40	Slave Clock (for 10 mc operation)	385.00
SM-40	Serial Memory (for 10 mc or 16 mc operation)	997.00
BL-40	H-BLOC chassis only (holds 40 H-PACs plus Slave Clock)	336.00
CU-40	Cooling Unit (One required per BL-40)	87.00
BP-40	Blank PAC	15.00
XP-40	PAC Extender	39.00
RP-40	Power Supply 4 Amp (for 1 H-BLOC)	475.00
RP-41	Power Supply 16 Amp (for 4 H-BLOCs)	767.00
RP-42	Power Supply 40 Amp (for 10 H-BLOCs)	1,185.00

PRICE LIST

effective date: November 1, 1961

Prices: F.O.B. Framingham, Massachusetts.
Terms: Net 30 days.
Delivery: From stock or as quoted.
Discounts: Quantity Discounts are applied on basis of total price of individual orders.
Individual Order Total $ 15,000.00 to $39,999.99 Less 5%
40,000.00 to 99,999.99 Less 10%
100,000.00 and up — discounts on request

Suggestions for ordering

Always order by catalog model number and name of product desired. Wherever possible, mention significant specifications to prevent misunderstanding- for example: *"H-BLOC, Model BL-40."*

Orders may be sent to either Framingham, Massachusetts or Los Angeles, California.

To communicate with 3C

	EASTERN DIVISION	WESTERN DIVISION
Mail:		
	983 Concord Street Framingham, Mass.	2251 Barry Avenue Los Angeles, Calif.
Telephone:		
	Area Code 617 CEdar 5-6220 (Bost.) 875-6185 (Fram.)	Area Code 213 GRanite 8-0481 BRadshaw 2-9135
TWX:	FRAM MASS 17	W LA CAL 6634

Western Union:

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Cable Address: Compcon, Framingham, Mass., U.S.A.

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(a) Under 20 pounds — Parcel Post

(b) 20 to 75 pounds — Railway Express

(c) Over 75 pounds — Truck or Carloading Company

For expedited service we will gladly ship by Air Freight, Air Express, Air Parcel Post, etc., as requested.

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A major area of specialization by *Computer Control Company, Inc.* (3C) is the design, development and manufacture of *special-purpose digital computers* and *systems.*

Further, 3C is also a leading supplier of *digital modules, magnetic core memory systems, SONILINES* (sonic delay lines), and *package test equipment.*

An abundance of literature describing these other areas of 3C proficiency is available by calling or writing to the address(es) listed below!

standard warranty

a) Computer Control Co., Inc., warrants all 3C products against defects in workmanship, materials, and construction under normal use and service for a period of ONE YEAR from the date of purchase except that liability for defective vacuum tubes, transistors, and germanium diodes shall conform and be limited to the obligations of the original manufacturer's warranties covering these components.

b) This warranty does not extend to any of our products which have been subjected to misuse, neglect, accident, or improper installation or application. Nor shall it extend to products which have been repaired or altered outside of our factory.

c) For service under this warranty, please advise the factory promptly of all pertinent details. Transportation charges covering return of defective products to our factory shall be at our expense if such products are determined to be defective within the limitations of this warranty. Computer Control Co., Inc. will repair or replace the defective product in accordance with its own best judgment.

d) Computer Control Co., Inc. requests immediate notification for any claims arising from damage in transit in order to determine if carrier responsibility exists.

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