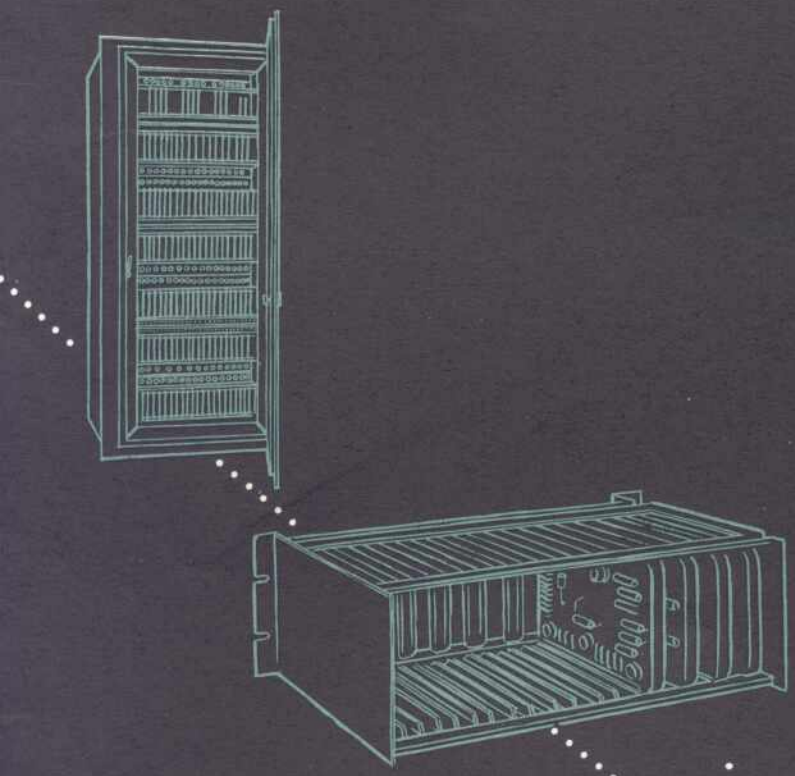
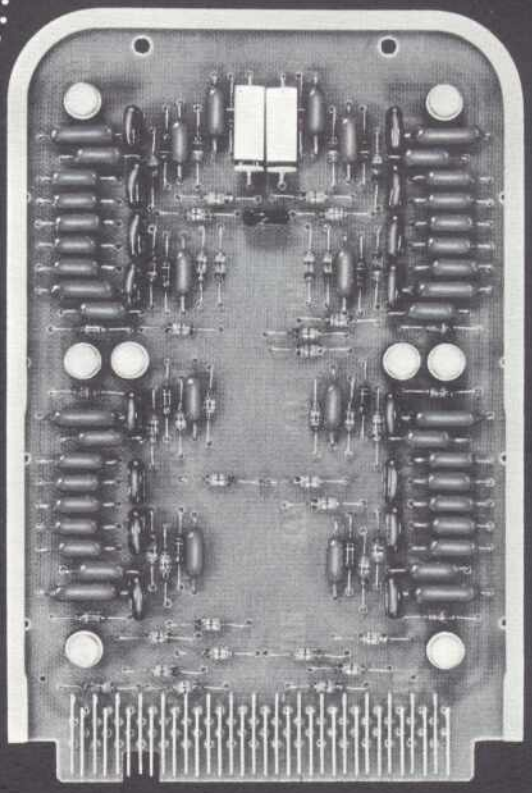
catalog **S**





SERIES S PACS

An integrated family
of digital modules for *dc*
to *one megacycle* operation.

COMPUTER CONTROL COMPANY, INC.

FRAMINGHAM, MASSACHUSETTS LOS ANGELES, CALIFORNIA

NEW *series of* S-PACS

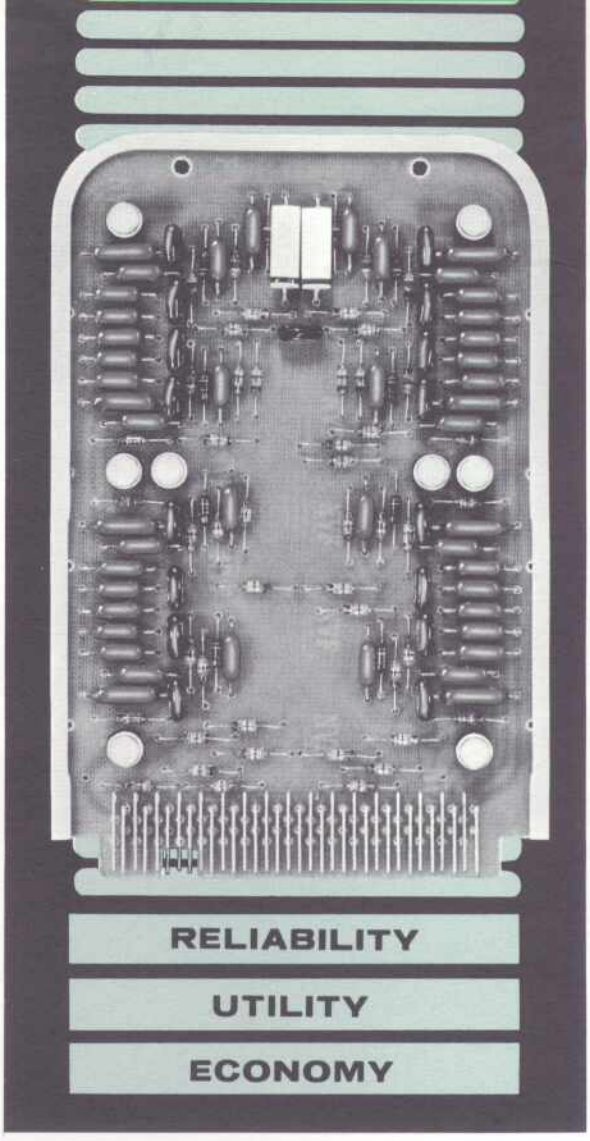
Computer Control Company is pleased to make available a *new* series of *S-PACs* for immediate use in your general or specialized application!

Designed for maximum RELIABILITY, UTILITY AND ECONOMY, these *S-PACs* offer outstanding technical performance and quality construction!

The result of a comprehensive design, development, and evaluation program, *S-PAC* circuit configurations are the optimum attainable based on the utilization of the most advanced components and techniques available!

For example, mechanical packaging of the Series S utilizes the *same proven physical formats, top grade materials,* and *quality assurance methods of production and assembly* which have gained widespread acceptance for Computer Control Company's V, M, T and MIL-T Series of 3C-PACs!®

The following categories of specific features and characteristics of the *3C-PAC Series S family* are presented for your consideration and evaluation:



logical.....

—S-PACs utilize *NAND* (not-and) logic. A simple set of rules are provided to permit the straightforward implementation of *AND-OR* logic or *NOR* logic directly with the basic S-PAC *NAND* modules. A number of valid and consistent logical systems can be created by using different combinatorial groupings of the basic logical operators *AND, OR, NOT,* etc. The most common systems are those using *AND-OR, NOT-OR,* and *NOT-AND* logic. None of these systems possess any inherent advantages or virtues relative to any or all of the others per se. It is the implementation of these systems of pure logic by practical electronic circuits that gives rise to virtues and deficiencies and these are always in terms of the circuits themselves. 3C has chosen *NAND* logic for its S-PAC family of modules because of the simplicity and usage symmetry of the resulting single circuit which is basic to all S-PAC modules. Most of the significant features and advantages which are listed in this literature are a direct consequence of this.

— All S-PACs are directly compatible with one another. No intermodule coupling networks or components are required.

— S-PACs will drive Computer Control Company's T-PACs* directly. T-PAC to S-PAC compatibility is obtained by a simple "marriage" S-PAC or by using the Model FS-10 PAC of the T Series.

— All *flip-flop* and *gating* S-PACs are extensions of the standard basic gate circuit. In fact, two gate circuits may be used "back-to-back" to form a flip-flop circuit equivalent to that of the FF-30 S-PAC.

— All *gates* will drive seven S-PAC unit loads.

— All *flip-flops* will drive six S-PAC unit loads from each side.

— All S-PAC AC inputs to a gate or flip-flop are expandable to ten by means of auxiliary diodes which are available on the gate PACs.

— All S-PAC DC inputs are similarly expandable to ten.

— Trailing edge triggering of flip-flops via the AC inputs permits reliable output gating of the input without intervening delay circuits.

** See 3C catalog T and supplementary bulletins.*

electrical.....

— Frequency range of operation is *DC* to one *megacycle.*

— *Output* signal levels are *0 volts* for logical ZERO and *−6 volts* for logical ONE.

— *Power supply* voltages are *+12 volts, −6 volts,* and *−18 volts.*

— All *inputs* are diode coupled/isolated.

— All *output* signals are clamped.

— All *input* noise rejection margins are *1.5 volts minimum.*

— All *outputs* are capable of driving a minimum of 400 micro microfarads of stray capacitance at the 1 mc frequency rate in addition to the specified number of S-PAC unit loads. This is equivalent to twenty-five feet of tightly cabled unshielded #22 wire.

— *Temperature range* of operation is *−20°C* to *+55°C.*

— All listed performance specifications are guaranteed minimums based upon "worst case" stack-up of tolerances. Actual performance specifications will invariably exceed these "worst case" minimums.

mechanical.....

— High component density is maintained throughout for maximum volumetric efficiency. Either *19* or *28 S-PACs* may be contained in the 19" x 5¼" x 9½" *S-BLOC* volume. At four flip-flops per *S-PAC* this gives a maximum total of 112 flip-flops in a single *S-BLOC.*

— Dip-soldered, etched circuits on glass-impregnated epoxy cards are utilized for *maximum uniformity, ruggedness,* and *dimensional stability.*

—All *S-PACs* have metal frames or handles to add rigidity to the card, and to facilitate proper guidance into the mating connector.

— Open construction of the *S-BLOC* is designed to permit natural convection cooling of the *S-PACs.* It also permits easy forced air cooling or venting of a stack of *S-BLOCs* if desired.

— Choice of taper pin or solder connectors are available on the *S-BLOCs.* Wire-wrap or printed circuit terminals can be supplied on special order.

reliability.....

— One basic transistor type is used throughout all *gating* and *flip-flop* circuits.

— A minimum number of passive component types and values is *incorporated* in the circuit design.

— All component types have been carefully selected and evaluated for *reliable* long life performance.

— *Precision* components are employed throughout, although circuits are designed for *non-precision* tolerances. *Resistors* are high-quality high-stability deposited carbon film type. *Capacitors* are molded Duramica.

— *Connectors* are *hermaphroditic* type with spring contact self-wiping action. Spring contact material is *phospor bronze with gold flash over nickel plating.*

— A rigid *inspection, testing,* and *overall quality assurance* program is an integral part of the *S-PAC* manufacturing process.

— *Preshipment burn-in* and/or *high temperature bakes* prior to final test and inspection are employed as required to eliminate incipient catastrophic component failures.

— *MTBF* probability data has been calculated for all *S-PACs.* Continuous life testing is being conducted to provide empirical corroboration of calculated data.

convenience.....

— Nineteen test point terminals are provided on the front of the *S-BLOC.* They may be wired to any desired signal locations in the *BLOC.*

— *PAC* type by *model number* and by *color code* is designated on the *S-PAC* handles.

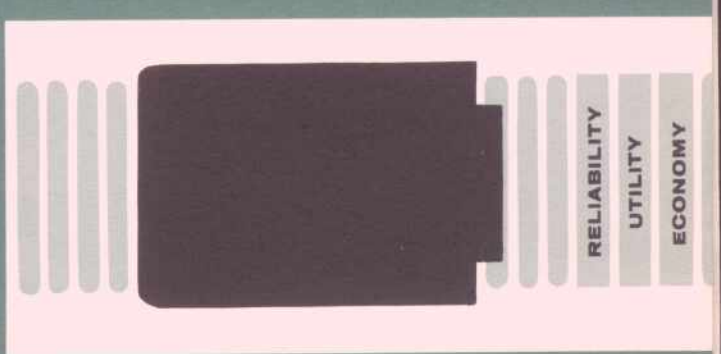
— All *S-PACs* are uniquely polarized to prevent improper insertion.

— Power busses and ground bus are factory prewired on all *S-BLOCs.*

— Power busses are protected to prevent accidental shorting.

— The connector mounting frame comprising the front of the *S-BLOC* may be *easily removed* from the *BLOC* as an integral unit to permit convenient bench wiring of system logic.

— A *PAC* retainer bar on the rear of the *S-BLOC* permits *BLOC* orientation in *any* position and affords *additional protection* against shock and vibration.



Basic Flip-Flop

MODEL

FF-30

This PAC contains four identical, independent, low-cost bistable elements for use as input-output registers, or for any logical application in which complementing, shifting, etc. is not required. Circuits are capable of operating from D.C. to 1 megacycle. One set and two reset inputs are provided and each of these is expandable to 10 inputs per side. The set and reset outputs are each capable of driving 6 S-PAC standard loads plus stray capacitance.

SPECIFICATIONS

Number of independent flip-flops per PAC:	4
Maximum Operating Frequency:	1 megacycle
Output Drive Capabilities:	6 unit loads per output
Input Loading:	1 unit load
Current Requirements per PAC:	
@ −18 V	83 ma
@ − 6 V	33 ma (reverse current into supply source)
@ +12 V	5 ma
Total PAC Power (Maximum):	1.1 Watts
Output Waveform Rise Time: (Typical)	0.1 microseconds
Output Waveform Fall Time: (Typical)	0.15 microseconds

Counter

MODEL

BC-30

This PAC contains four independent one megacycle counter stages which may be wired for binary or binary-coded-decimal operation. Internally wired logic allows 8421 BCD counting as well as divide by 5 and various other feedback counting modes. Preset operation of the counter is provided in all of the modes. The BC-30 may be wired for Up-Down counting or instantaneous carry operation in any of its modes by use of external S-PAC logic.

Each stage has a complement input which features built-in trailing edge triggering. This allows the counter output to be gated with a count signal without need for delay circuits or two-phase clocks. The set and reset outputs of each stage are each capable of driving six S-PAC standard loads plus stray capacitance.

SPECIFICATIONS

Number of flip-flop stages per PAC:	4
Maximum Counting Rate:	1 megacycle
Output Drive Capabilities:	6 unit loads per output
Input Loading:	DC Input — 1 unit load Common Reset — 4 unit loads Complement — 2 unit loads
Current Requirements per PAC:	
@ −18 V	120 ma
@ − 6 V	29 ma (reverse current into the supply source)
@ +12 V	5 ma
Total PAC Power (maximum):	2.0 watts
Output Waveform Rise Time: (Typical)	0.1 microseconds
Output Waveform Fall Time: (Typical)	0.15 microseconds
Typical Carry Delay:	0.15 microseconds

Shift Register

MODEL

SR-30

This PAC is a prewired four-stage shift register which can shift at any rate up to and including one megacycle. It is designed to operate in all modes; serial-parallel, parallel-serial, and serial-serial.

Set and Reset inputs are provided for parallel loading of information. A common reset input is provided for simultaneously clearing all stages. The shift input features built-in trailing edge triggering. This allows the output of the register to be gated with the shift signal without need for delay circuits or two-phase clocks. The first stage of each register has a set and reset level control input for serial information entry. The set and reset outputs from each stage are capable of driving 6 S-PAC Standard Loads plus stray capacitance.

SPECIFICATIONS

Number of flip-flop stages per PAC:	4
Maximum Shift Rate:	1 megacycle
Output Drive Capabilities:	6 unit loads per output
Input Loading:	DC Input — 1 unit load Common Reset — 4 unit loads Shift Pulse — 7 unit loads Level Control — ¼ unit load
Current Requirements per PAC:	
@ −18 V	113 ma
@ − 6 V	29 ma (reverse current into the supply source)
@ +12 V	5 ma
Total PAC Power (maximum):	1.9 watts
Output Waveform Rise Time: (Typical)	0.1 microseconds
Output Waveform Fall Time: (Typical)	0.15 microseconds

Universal Flip-Flop

MODEL

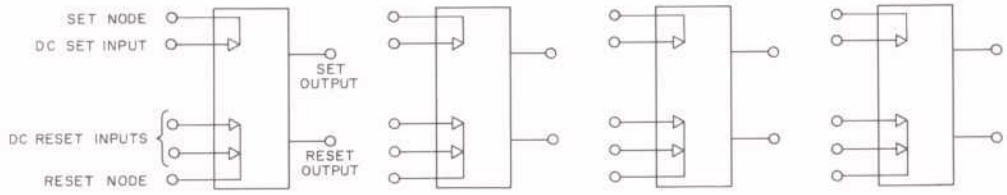
UF-30

This PAC contains two identical independent flip-flops which can perform all the functions of the other S-PAC flip-flops, with provision for many other logical functions as well. Provision of two sets of AC inputs allows the UF-30 to be wired as a left-right shift register or as a binary counter and shift register simultaneously.

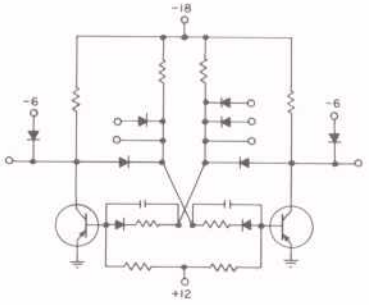
Each stage has available direct-coupled set and reset inputs which can be used for parallel loading of information. In addition, each stage has three AC coupled inputs. One is common to both set and reset and can be wired for either complementing or shifting. The other two AC inputs with their associated level control inputs provide independent set and reset gates on each stage. The set and reset outputs are each capable of driving 6 S-PAC standard loads plus stray capacitance.

SPECIFICATIONS

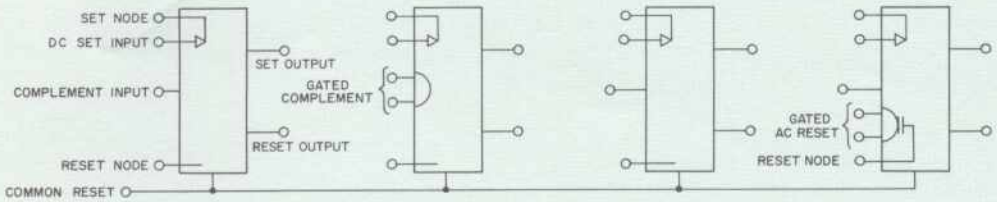
Number of independent flip-flops per PAC:	2
Maximum Operating Frequency:	1 megacycle
Output Drive Capabilities:	6 units loads per output
Input Loading:	DC Input — 1 unit load AC Input — 2 unit loads Level Controls — ¼ unit load
Current Requirements per PAC:	
@ −18 V	82 ma
@ − 6 V	28 ma (reverse current into supply source)
@ +12 V	3 ma
Total PAC Power (maximum):	1.4 Watts
Output Waveform Rise Time: (Typical)	0.1 microseconds
Output Waveform Fall Time: (Typical)	0.15 microseconds



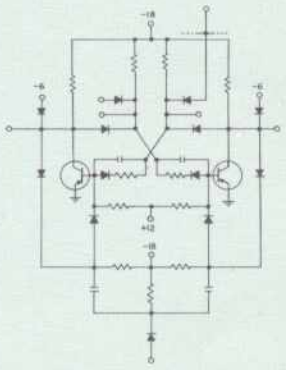
FF-30 BLOCK DIAGRAM



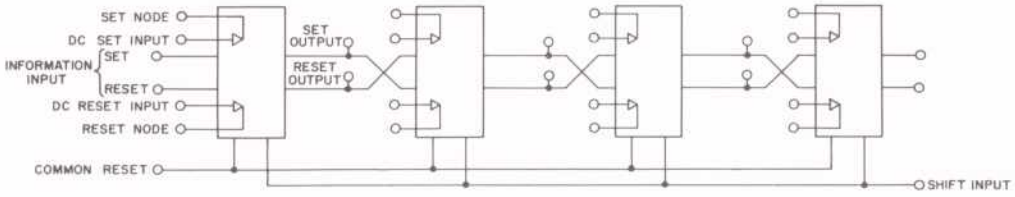
FF-30 TYPICAL SCHEMATIC



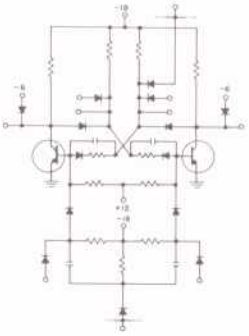
BC-30 BLOCK DIAGRAM



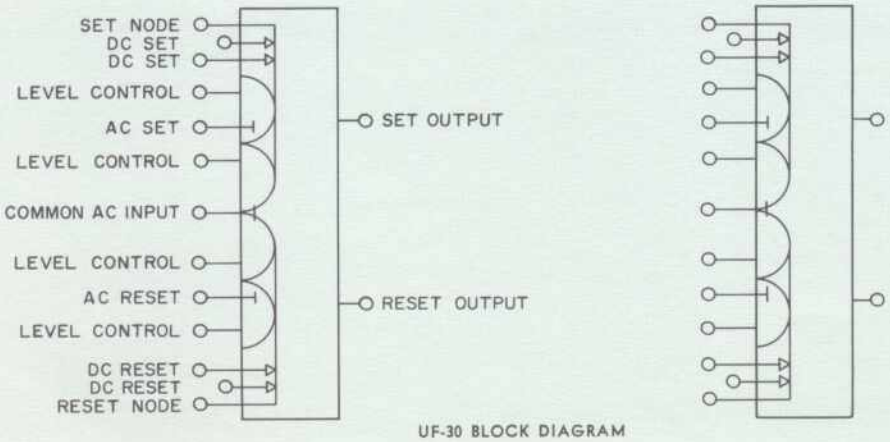
BC-30 TYPICAL SCHEMATIC



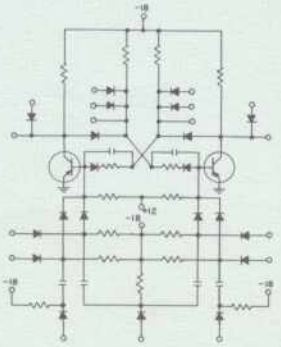
SR-30 BLOCK DIAGRAM



SR-30 TYPICAL SCHEMATIC



UF-30 BLOCK DIAGRAM



UF-30 TYPICAL SCHEMATIC

S-PACS

Gate PAC

MODEL DN-30

This PAC contains four expandable S-PAC NAND gates, plus diodes to implement the expansion. Each gate has available two prewired diode inputs. The additional diodes are grouped into two three-diode and two two-diode gate clusters and may be wired to increase the number of gate inputs. As an example, the components provided on one DN-30 PAC allow it to be wired as two five-input gates and two four-input gates.

An S-PAC NAND gate will perform either the function AND or OR depending on the polarity of the information. It will gate levels, pulses, or a combination of each. It will operate at speeds from dc to one megacycle and is capable of driving seven S-PAC standard loads plus stray capacitance.

SPECIFICATIONS

Number of independent circuits per PAC:	4 two-input gates plus, (for gate expansion) 2—two-diode clusters 2—three-diode clusters
Maximum Operating Frequency:	1 megacycle
Output Drive Capability:	7 unit loads
Input Loading:	1 unit load
Current Requirements per PAC:	
@ −18 V	45 ma
@ − 6 V	25 ma (reverse current into supply source)
@ +12 V	3 ma
Total PAC Power (maximum):	.8 watts
Output Waveform Rise Time: (Typical)	0.1 microseconds
Output Waveform Fall Time: (Typical)	0.15 microseconds
Maximum Circuit Delay:	0.1 microseconds

Inverter PAC

MODEL DI-30

This PAC contains eight expandable S-PAC NAND gates. Each gate has available two prewired inputs and may be expanded by wiring external diodes. Each gate performs identically to the DN-30 gates.

Two S-PAC NAND gates wired back-to-back form an S-PAC flip-flop; hence, pairs of unused gates may be wired as storage elements.

SPECIFICATIONS

Number of independent circuits per PAC:	8 expandable 2-input gates
Maximum Operating Frequency:	1 megacyle
Output Drive Capability:	7 unit loads
Input Loading:	1 unit load
Current Requirements per PAC:	
@ −18 V	88 ma
@ − 6 V	48 ma (reverse current into supply source)
@ +12 V	5 ma
Total PAC Power (maximum):	1.6 watts
Output Waveform Rise Time: (Typical)	0.1 microseconds
Output Waveform Fall Time: (Typical)	0.15 microseconds
Maximum Circuit Delay:	0.1 microseconds

Delay Multivibrator Pulse Shaper

MODEL DM-30

This PAC contains three independent monostable (one-shot) multivibrators capable of generating pulses in a variety of widths. Internally provided capacitors may be wired for pulses from 0.7 to 200 μsec in width. If externally mounted capacitors are used, pulse widths of several seconds may be obtained. Each multivibrator has available a trigger input and bipolar outputs. The assertion and negation outputs are each capable of driving four S-PAC standard loads. The DM-30 is useful in applications calling for delayed levels or pulse shaping and standardizing.

SPECIFICATIONS

Number of independent MV's per PAC:	3
Maximum Operating Frequency:	500 kc
Output Drive Capabilities:	4 units loads per output
Input Loading:	2 unit loads
Internal Pulse Widths:	0.7, 10 or 200 μ sec
Current Requirements per PAC:	
@ −18 V	115 ma
@ − 6 V	29 ma (reverse current into supply source)
@ +12 V	3 ma
Total PAC Power (maximum):	1.2 watts
Output Waveform Rise Time: (Typical)	0.1 microseconds
Output Waveform Fall Time: (Typical)	0.15 microseconds
Recovery Time:	80% of pulse width

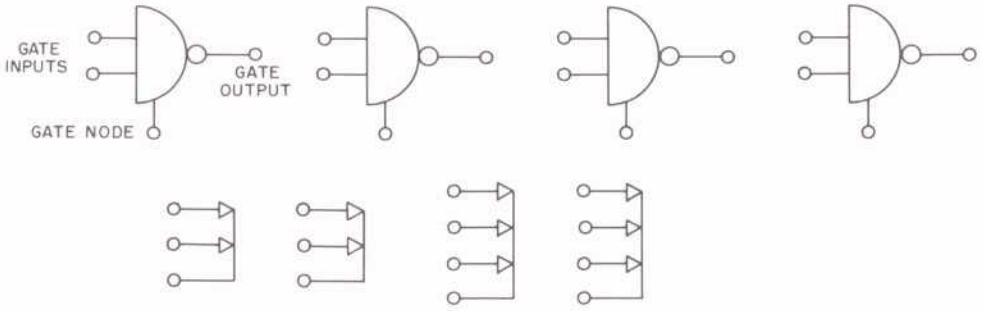
Adjustable Delay Multivibrator

MODEL DM-30A

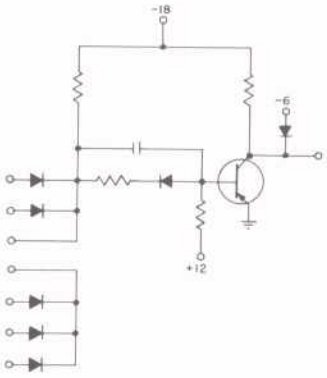
This PAC is essentially similar to the DM-30. In addition to the performance of the DM-30, the DM-30A provides a means of continuously varying or trimming pulse width. Potentiometers are mounted directly on the PAC for this purpose. The negation output of the DM-30A can drive four S-PAC standard loads plus stray capacitance, and the assertion output can drive one S-PAC standard load. This PAC is useful in applications calling for precise pulse width control.

SPECIFICATIONS

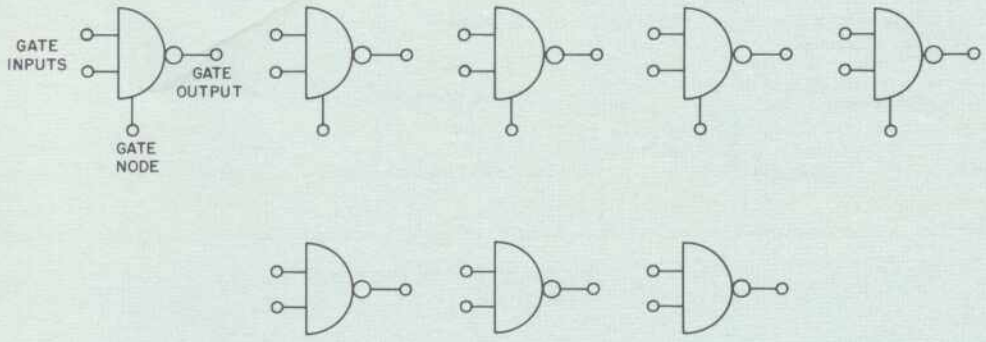
Number of Independent MV's per PAC:	3
Maximum Operating Frequency:	500 kc
Output Drive Capabilities:	Assertion output: 1 unit load Negation output: 4 unit loads
Input Loading:	2 unit loads
Pulse Width:	Nominal delays same as DM-30, variable over a range of 5:1 from 6/10 of nominal to 3 times nominal delay.
Current Requirements per PAC:	
@ −18 V	110 ma
@ − 6 V	29 ma (reverse current into supply source)
@ +12 V	3 ma
Total PAC Power (Maximum):	1.9 watts
Output Waveform Rise Time: (Typical)	0.1 microseconds
Output Waveform Fall Time: (Typical)	0.15 microseconds
Recovery Time:	80% of pulse width



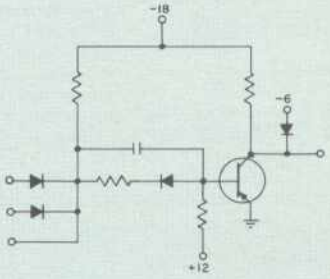
DN-30 BLOCK DIAGRAM



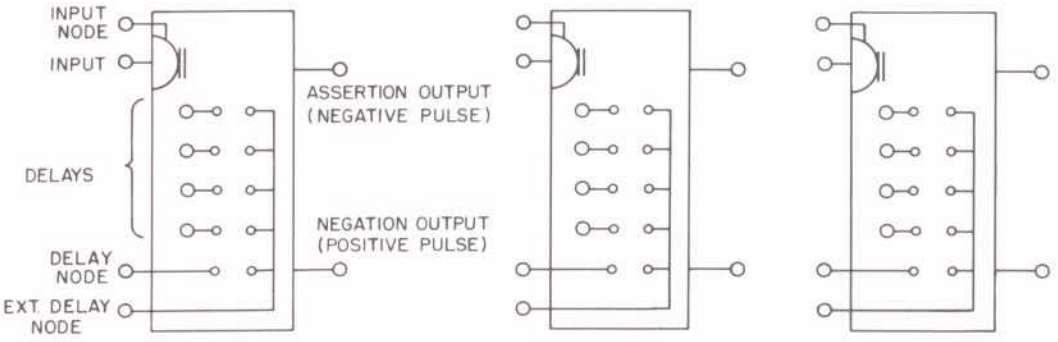
DN-30 TYPICAL SCHEMATIC



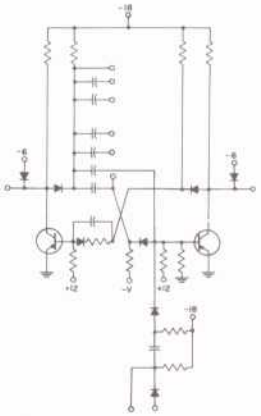
DI-30 BLOCK DIAGRAM



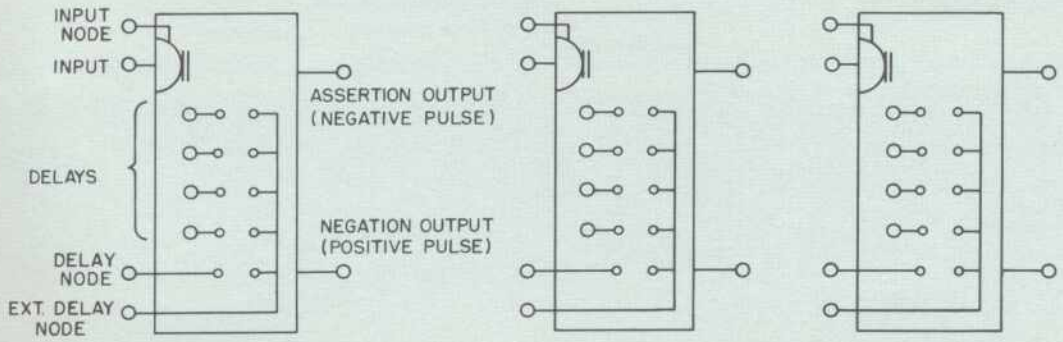
DI-30 TYPICAL SCHEMATIC



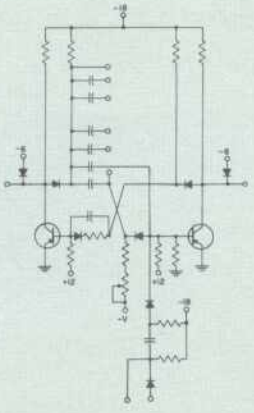
DM-30 BLOCK DIAGRAM



DM-30 TYPICAL SCHEMATIC



DM-30A BLOCK DIAGRAM



DM-30A TYPICAL SCHEMATIC

S-PACS

Diode Pac

MODEL

DC-30

This PAC contains diodes plus one expandable S-PAC NAND gate. The diodes include five three-diode and two two-diode clusters and may be wired to expand the inputs to other S-PAC circuits; i.e. gates, flip-flops, power amplifiers, etc. The gate has available two pre-wired inputs and performs identically to the DN-30-gates.

SPECIFICATIONS

Number of independent circuits per PAC:	1 two-input gate, plus (for gate expansion) 5 — three-diode clusters 2 — two-diode clusters
Maximum Operating Frequency:	1 megacycle
Output Drive Capability:	7 unit loads
Input Loading:	1 unit load
Current Requirements per PAC:	
@ −18 V	10 ma
@ − 6 V	6 ma (reverse current into supply source)
@ +12 V	0.5 ma
Total PAC Power (maximum):	0.19 watts
Output Waveform Rise Time: (Typical)	0.1 microseconds
Output Waveform Fall Time: (Typical)	0.15 microseconds
Maximum Circuit Delay:	0.1 microseconds

Free-Running Multivibrator

MODEL

MV-30

This PAC contains one free-running variable frequency multivibrator capable of operating at frequencies from 500 cycles per second to one megacycle in five increments of range. Ranges are determined by RC networks contained on the S-PAC. Range selection is performed by jumper wiring on the connector to select the appropriate networks. This may be done either by permanent wiring for a set range or by toggle switches. Continuously variable control within each range is by a miniature potentiometer mounted on the MV-30. This may be replaced by an external potentiometer for remote control if desired. The MV-30 includes a built-in control gate for on-off control. A sync output is provided for synchronous gating. Both assertion and negation outputs are available and each is capable of driving 12 S-PAC unit loads. The output pulse width may be set at 0.6, 2, or 5 microseconds.

SPECIFICATIONS

Frequency Range:	500 cps to 1 mc in five ranges
Output Drive Capabilities:	Assertion — 12 unit loads Negation — 12 unit loads Sync — 1 unit load
Input Loading:	Start control — 7 unit loads Gate control — 7 unit loads
Pulse Width:	.6 microsecond standard, optional 2 or 5 microseconds at lower frequency
Current Requirements per PAC:	
@ −18 V	130 ma
@ − 6 V	15 ma (reverse current)
@ +12 V	7 ma
Total PAC Power (Maximum):	2.3 watts

Master Clock

MODEL

MC-30

This PAC contains one crystal controlled clock circuit capable of operating at any crystal frequency within the range 100 kc to 1 megacycle. With the crystal removed, the MC-30 may be driven from an external frequency source (e.g. a T-PAC clock). The MC-30 provides a built-in control gate for turning the clock on and off. A SYNC output is provided for coherently controlling the gating action to prevent pulse splitting. Both assertion and negation outputs are available and each is capable of driving 12 S-PAC unit loads. The output pulse width may be set at 0.6, 2, or 5 microseconds.

SPECIFICATIONS

Frequency Range:	100 kc to 1 mc crystal controlled
Output Drive Capabilities:	Assertion — 12 unit loads Negation — 12 unit loads Sync — 1 unit load
Input Loading:	Gate control — 1 unit load
Pulse Width:	.6 microsecond standard, optional 2 or 5 microseconds at lower frequencies
Current Requirements per PAC:	
@ −18 V	70 ma
@ − 6 V	5 ma (reverse current into supply source)
@ +12 V	13 ma
Total PAC Power (Maximum):	1.4 watts

Solenoid Driver

MODEL

SD-30

This PAC contains four independent solenoid driver circuits. Each is capable of providing up to one half amp of solenoid current from a minus 48 volt d.c. supply voltage or up to one ampere from a minus 28 volt source. Any negative voltage up to 48 volts may be used. Each input represents two S-PAC unit loads.

SPECIFICATIONS

Number of independent solenoid drivers per PAC:	4
Output Drive Capabilities:	1 amp at −28 V ½ amp at −48 V
Input Loading:	2 unit loads
Damping:	Internal diode and 10 ohm resistor provided for damping overshoot.
Current Requirements per PAC:	
@ −18 V	200 ma
@ − 6 V	0 ma
@ +12 V	12 ma
Plus external solenoid current	
Total PAC Power (Maximum):	3.7 watts

Power Amplifier

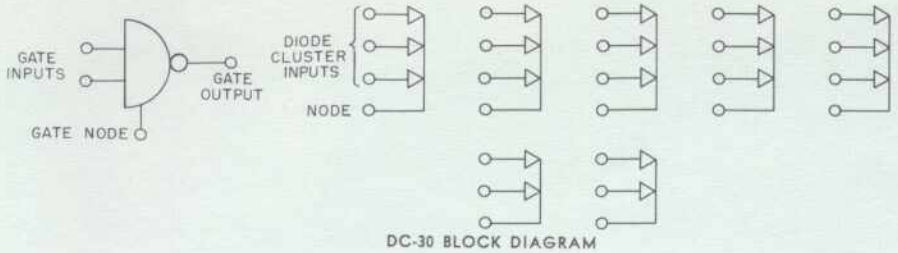
MODEL

PA-30

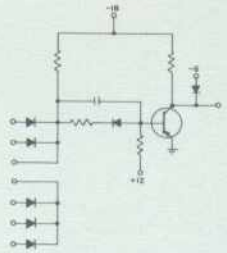
This PAC contains four independent power amplifiers capable of operating at speeds from dc to one megacycle. Each power amplifier has one input and two isolated outputs. Each of the two outputs is capable of driving 14 S-PAC standard loads plus stray capacitance. This PAC is useful for heavy load applications, such as driving shift lines, common reset lines, extra long information leads, etc.

SPECIFICATIONS

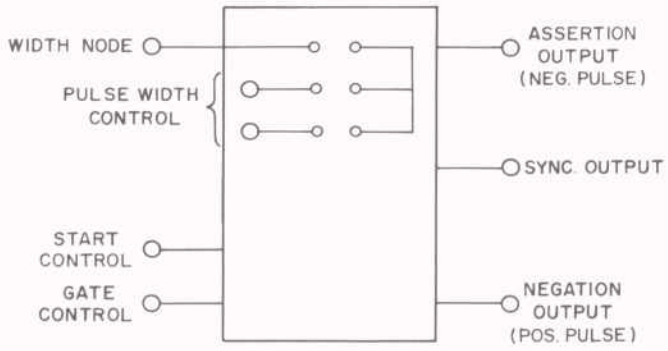
Number of independent pulse amplifiers per PAC:	4
Maximum Operating Frequency:	1 mc
Output Drive Capabilities:	28 unit loads per circuit
Input Loading:	3 unit loads
Current Requirements per PAC:	
@ −18 V	70 ma
@ − 6 V	21 ma (reverse current)
@ +12 V	10 ma
Total PAC Power (Maximum):	1.5 watts
Output Waveform Rise Time: (Typical)	0.1 microseconds
Output Waveform Fall Time: (Typical)	0.15 microseconds
Maximum Circuit Delay:	0.15 microseconds



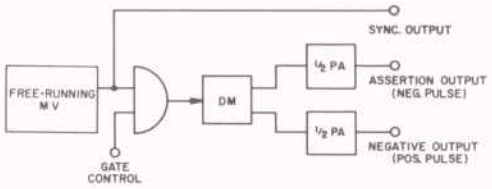
DC-30 BLOCK DIAGRAM



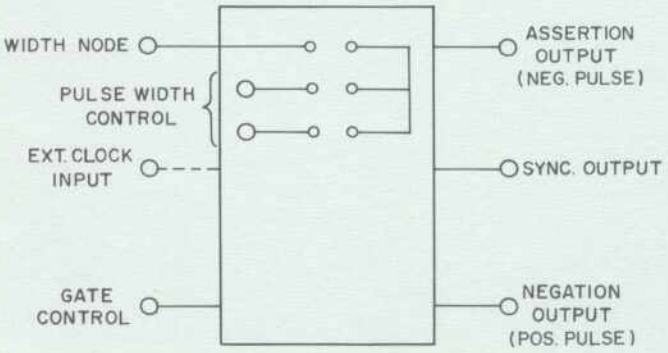
DC-30 TYPICAL SCHEMATIC



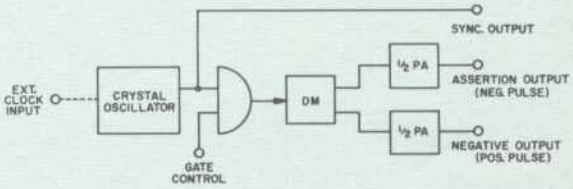
MV-30 BLOCK DIAGRAM



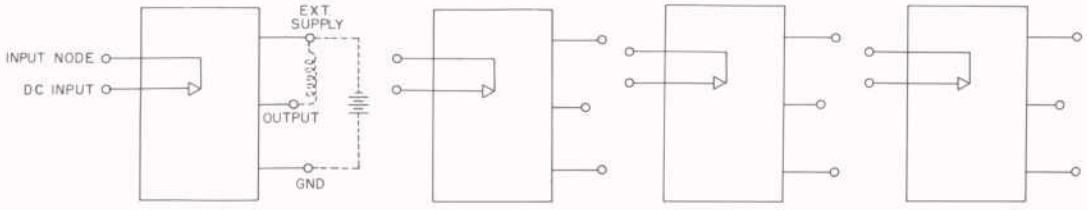
MV-30 FUNCTIONAL DIAGRAM



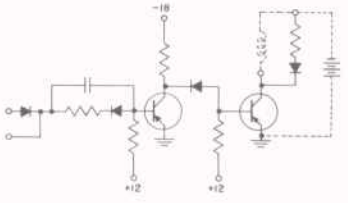
MC-30 BLOCK DIAGRAM



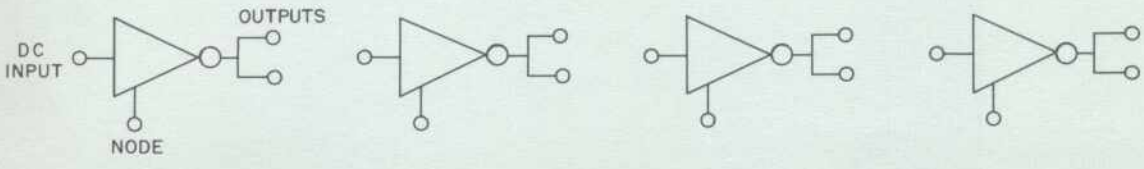
MC-30 FUNCTIONAL DIAGRAM



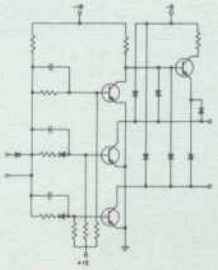
SD-30 BLOCK DIAGRAM



SD-30 TYPICAL SCHEMATIC



PA-30 BLOCK DIAGRAM



PA-30 TYPICAL SCHEMATIC

S-PACS

Neon Indicator

MODEL

UI-10

The Unit Indicator, Model UI-10 will display the state of any S-PAC flip-flop or of T-PAC Models LE-10 or FS-10. It also contains provision for driving an external indicator. Power required: −90 volts, 1 ma minimum to 2.3 ma maximum. Input requirements: −12 volts, at 0.2 ma from the FS-10; or 1 megacycle pulses −3 volts minimum amplitude from the LE-10, or −6 volts from any S-PAC flip-flop circuit.

Low Voltage Neon Indicator

MODEL

UI-30

A UI-30 will indicate the state of any flip-flop in the S-PAC series. It utilizes the standard minus 18 volts required for the other S-PACs. Indication is provided by a neon lamp. Base terminals are taper pin type which may also be used as solder receptacles. Current drawn from the −18 volt supply source is 3.0 ma maximum.

The UI-10 and UI-30 indicators have the following dimensions. Physical diameter is 13/32 inches. Minimum mounting spacing is 19/32 inches on centers. Overall length is 2 inches.

The Blank S-PAC

MODEL

BP-30

The blank S-PAC, Model BP-30 is a standard S-PAC card with etched power and ground busses from the appropriate connector terminals around its periphery. The bulk of the card is blank for the convenient mounting of any special circuits or components as desired by means of standard turret lugs and point-to-point wiring. Drilling, lugging, and point-to-point wiring of components and circuits do not require special skills and are easily performed.

PAC Extender

MODEL

XP-30

The function of the PAC Extender is to provide unobstructed access to any PAC while it is still electrically mounted in its appropriate S-BLOC Connector. The connector terminals on the front end of the XP-30 will mount into any S-BLOC connector and the connector on the rear of the XP-30 will accept the S-PAC which it is displacing. Front and rear terminals are directly tied together electrically.

power supplies.....

Three standard S-PAC Power Supplies are available. They utilize solid state circuits throughout. Regulation, stability, ripple, transient response, etc., are conservatively specified to meet the requirements of any S-PAC system. Initial voltage adjustments are made by means of internal locking set screws. Long term voltage stability precludes the need for periodic adjustments during usage. All components are derated for long reliable operation.

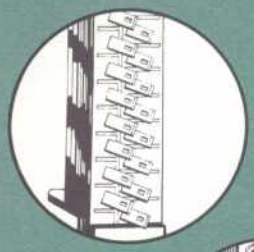
RELIABILITY
UTILITY
ECONOMY

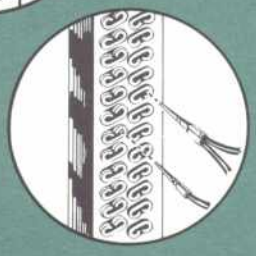
FORTHCOMING ADDITIONS TO THE S-PAC SERIES

Schmitt Trigger PAC, Model ST-30
BCD to Decimal Converter, Model BD-30
Binary to Octal Converter, Model BO-30
Magnetic Shift Register PAC, Model MR-30
Digital to Analog Ladder Network, Model LN-30
Cross-Over Detector, Model CD-30
Direct Coupled Amplifier, Model DA-30
Synchronizer, Model SP-30

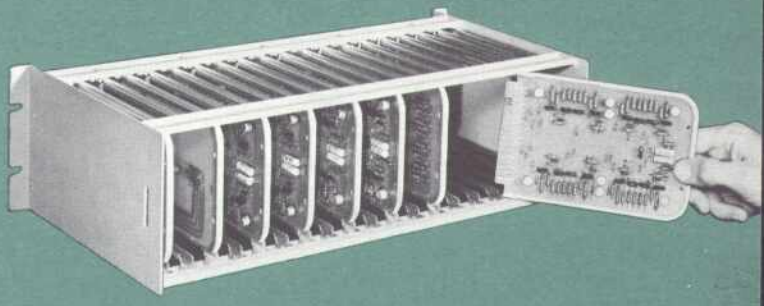
Plus "Marriage" PACs to provide complete compatibility with 3C-PACs Series T and Series H.

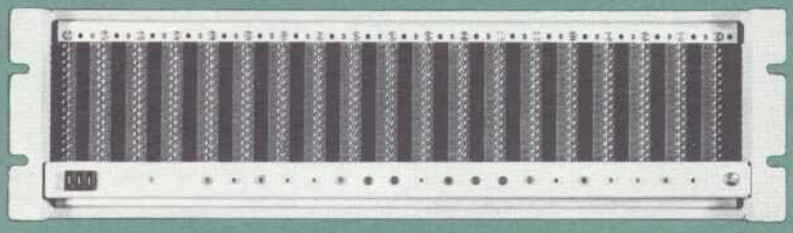
S-BLOCS





Illustrated at the left are two types of connections — Solder Pin and Taper Pin — either type is available!





There are four S-BLOC models available. All four models utilize the same basic structure, differing only in the type and number of connectors. Connectors are available with either solder terminals or taper pin terminals and S-BLOCs may be specified with 19 or 28 connectors of either type. S-BLOC construction is of the open type to permit convective air flow. In general, forced air cooling of S-PACs in the S-BLOC is not required. However, when 28-connector S-BLOCs are stacked in enclosed racks and filled with high dissipation circuits it may be desirable to provide air flushing by electric fan or blower. The open S-BLOC construction facilitates this as well.

S-BLOC construction is welded steel. Finish is textured, high durability vinyl enamel on a bonderized base. Many additional features of S-BLOCs are described under the MECHANICAL heading at the introduction to this catalog.

PRICE LIST *effective date: September 25, 1960*

HIGH-SPEED, STATIC, 1 MEGACYCLE, PLUG-IN DIGITAL MODULES

MODEL	DESCRIPTION	UNIT PRICE
FF-30	Basic Flip-flop (4 circuits)	$ 76.00
BC-30	Counter (4 stages)	96.00
SR-30	Shift Register (4 stages)	96.00
UF-30	Universal Flip-flop (2 circuits)	69.00
DC-30	Diode PAC (1 gate plus auxiliary diode clusters)	39.00
DN-30	Gate PAC (4 gates plus auxiliary diode clusters)	52.00
DM-30	Delay Multivibrator/Pulse Shaper (3 circuits)	97.00
DM-30A	Variable Delay Multivibrator (3 circuits)	127.00
DI-30	Inverter (8 circuits)	76.00
MV-30	Free-running Multivibrator	98.00
MC-30	Master Clock Oscillator	109.00
SD-30	Solenoid Driver	98.00
UI-10	Unit Indicator	7.50
UI-30	Unit Indicator (low voltage)	11.50
PA-30	Power Amplifier (4 circuits)	122.00
BP-30	Blank S-PAC	13.00
XP-30	PAC Extender	39.00
BL-30	S-BLOC (19 solder pin connectors)	139.00
BL-31	S-BLOC (19 taper pin connectors)	196.00
BL-32	S-BLOC (28 solder pin connectors)	168.00
BL-33	S-BLOC (28 taper pin connectors)	265.00
RP-30 RP-31 RP-32	Power Supply — 2.0 Amps Power Supply — 8.0 Amps Power Supply — 20.0 Amps	

See section below for discount policy

DISCOUNTS

Quantity discounts are applied on the basis of the total price of each individual order as follows:

Individual Order Total	Discount
$ 5,000.00 to $ 14,999.99	Less 5%
$ 15,000.00 to $ 29,999.99	Less 10%
$ 30,000.00 to $100,000.00	Less 15%
$100,000.00 and over	On request

No trade, O.E.M., educational, or other special discounts are available. 3C adheres rigidly to the policy of equally favored treatment to all customers.

TERMS

Domestic terms are net 30 days. All prices are quoted F.O.B. Factory and are subject to change without notice.

Suggestions for ordering

Always order by catalog model number and name of product desired. Wherever possible, mention significant specifications to prevent misunderstanding - for example: *"S-BLOC, Model BL-30, 19 connectors, solder pin terminals."*

Orders may be sent to either Framingham, Massachusetts or Los Angeles, California.

To communicate with 3C

	Eastern Division	Western Division
Mail:	983 Concord Street Framingham, Mass.	2251 Barry Avenue Los Angeles, Calif.
Telephone:	CEdar 5-6220 (Boston) TRinity 5-6185 (Fram.)	GRanite 8-0481 BRadshaw 2-9135
TWX:	FRAM MASS 17	W LA CAL 6634

Western Union: *Direct telegram printer communications with Western Union are maintained for prompt handling of messages.*

Shipments

Except when specified otherwise, shipments are generally made as follows:

(a) Under 20 pounds — Parcel Post

(b) 20 to 75 pounds — Railway Express

(c) Over 75 pounds — Truck or Carloading Company

For expedited service we will gladly ship by Air Freight, Air Express, Air Parcel Post, etc., as requested.

standard warranty

a) Computer Control Co., Inc., warrants all 3C products against defects in workmanship, materials, and construction under normal use and service for a period of ONE YEAR from the date of purchase except that liability for defective vacuum tubes, transistors, and germanium diodes shall conform and be limited to the obligations of the original manufacturer's warranties covering these components.

b) This warranty does not extend to any of our products which have been subjected to misuse, neglect, accident, or improper installation or application. Nor shall it extend to products which have been repaired or altered outside of our factory.

c) For service under this warranty, please advise the factory promptly of all pertinent details. Transportation charges covering return of defective products to our factory shall be at our expense if such products are determined to be defective within the limitations of this warranty. Computer Control Co., Inc. will repair or replace the defective product in accordance with its own best judgment.

d) Computer Control Co., Inc. requests immediate notification for any claims arising from damage in transit in order to determine if carrier responsibility exists.

3C

COMPUTER CONTROL COMPANY, INC.

EASTERN DIVISION: 983 Concord Street • Framingham • Massachusetts
TRinity 5-6185, CEdar 5-6220 — TWX: FRAM MASS 17

WESTERN DIVISION: 2251 Barry Avenue • Los Angeles 64 • California
GRanite 8-0481, BRadshaw 2-7137 — TWX: West LA CAL 6634

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