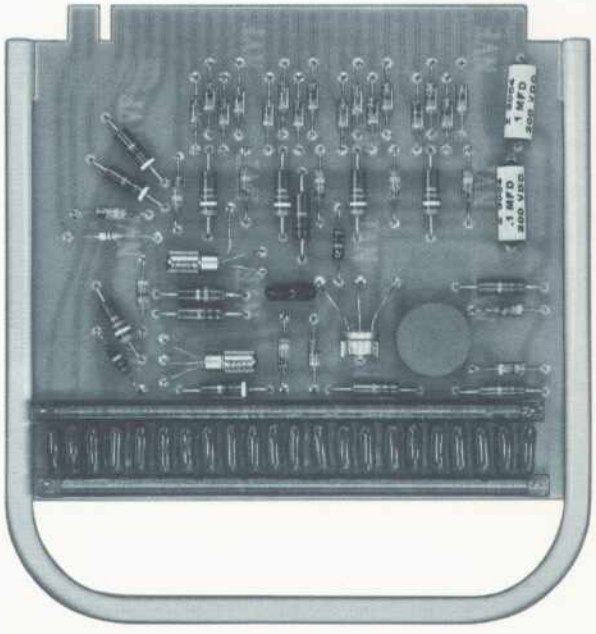
Catalog T

SERIES T PACS

DIGITAL MODULES
ONE MEGACYCLE
SYNCHRONOUS LOGIC



COMPUTER CONTROL COMPANY, INC.
FRAMINGHAM, MASS., LOS ANGELES, CALIF.

INTRODUCTION

Computer Control Company's *Series T family of 3C PACs* has received widespread acceptance and critical acclaim from digital systems designers! They are now in use in a notable variety of installations *throughout the world!* There are *T-PAC* systems in *mobile vans, aboard naval vessels,* and *aloft in aircraft!* Numerous *other* important commercial installations are also being implemented with *T-PACs!*

To enhance the established reliability of the *T-PAC* series, a *continuing* program of improvement and updating is being maintained in phase with progress in the state of the art! As a result, *T-PACs* now provide *all* of the benefits of new developments *plus* the many advantages derived from established usage and experience!

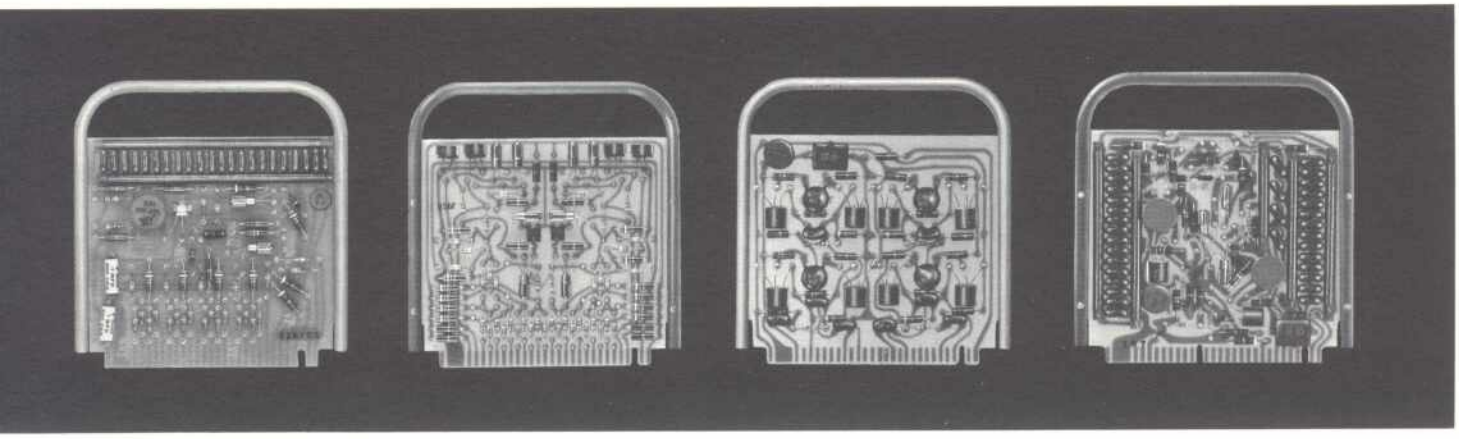
Another significant feature is that *additional* PAC types have been and are being continuously introduced so that *T-PACs* now represent *one of the most complete and comprehensive* families of digital modules available! The purpose of this new brochure is to present the *complete* family of *T-PACs* and *T-PAC accessories* under one cover.

GENERAL

Following are the various categories of features and characteristics which describe the Series T family:

LOGICAL

1. T-PACs utilize synchronous logic in the convenient *AND-OR-NOT* format.
2. A single *Logical Element* of the T-PAC family *(Model LE-10)* is capable of implementing all functions of three binary variables and the majority of four and five variable functions.
3. The *ASSERTION* and *NEGATION* outputs of the *Logical Element* are each capable of driving 20 T-PAC unit loads (gate inputs) directly.
4. T-PAC output signals are automatically maintained in precise synchronism with the system master clock. Signal phasing problems are non-existent.
5. The SM-10 *Serial Memory Unit* provides compact, convenient, reliable memory storage with capacity up to 1500 bits in one plug-in package.
6. The one word line *WL-10* memory provides convenient, economical, fast access, short loop storage capabilities in capacities up to 40 bits plus logical capability.
7. The one pulse period electrical delay lines *(DP-10 and DU-10)* provide convenient means for serial-to-parallel and parallel-to-serial conversion of information trains. They are also useful to implement circulating memory loops with multi-tap provisions.
8. For large capacity, fast access memories, *Computer Control Company's TCM series* of high speed random access magnetic core memories are directly com-



CHARACTERISTICS

patible with T-PACs physically and electrically.

9. The overall T-PAC concept has been carefully devised to afford ease of system design and equipment minimization for the logical designer in accordance with the techniques of Boolean* algebra.

ELECTRICAL

1. Basic clock frequency is *one megacycle.*
2. Output waveforms of the *Logical Element* T-PAC *(LE-10)* are completely independent of the inputs with respect to amplitude, duration, rise time, fall time, and clock phasing within the pulse period. The *GO:NO-GO* transfer characteristic of the *LE-10* amplifier circuit eliminates signal deteriorations with respect to waveform and timing irrespective of the number of PACs in the signal path.
3. *Logical Element* output signal levels are *4 volts at a 91 ohm impedance level.* Signal-to-noise ratio is *better* than *10 to 1.*
4. Inter-package signal connections employ *open wiring.* Cross-talk problems are eliminated by the *low impedance level.*
5. A single power supply voltage at *−16 volts* is employed.
6. Conservative noise rejection margins are built into each T-PAC circuit.
7. Temperature range of operation is *0°C to +55°C.*

*NOTE: *"Symbolic Logic, Boolean Algebra and the Design of Digital Systems" by the technical staff of Computer Control Company, Inc. provides an illustrated basic text on the utilization of these techniques. Copies are available on request.*

MECHANICAL

1. Overall PAC dimensions are *5"* by *5".*
2. Overall BLOC dimensions are *5½" high* by *19" wide* by *8" deep.*
3. T-PACs utilize *dip soldered, etched* circuits on a glass impregnated epoxy laminate for maximum uniformity, dimensional stability, and ruggedness.
4. A full tubular PAC frame serves as a handle and also improves slot guidance into the connector.
5. A gold plated tuning fork type of etched circuit connector mates with the solder-plated etched fingers on the PACs. Rigid quality control and careful inspection of dimensional tolerances provides a PAC-to-connector electrical union that has proven reliable in all applications.
6. All transistors are *clip mounted* to retain maximum lead lengths.
7. All semi-conductors are *wired through eyelets* for ease of replacement.
8. All components are mounted on *a single side.*

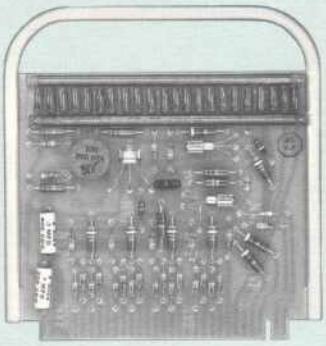
CONVENIENCE

1. Signal inter-wiring utilizes *taper pins* for rapid and reliable electrical connections and ease of re-wiring.
2. *Clock, power,* and *ground* busses are factory pre-wired and are enclosed by the transverse bezels on the 3C BLOC.
3. Only *logical signal input* and *output terminals* are accessible on the 3C BLOC plugboard. Circuits are designed to avoid *potential damage* due to wiring errors or accidental shorts.
4. A plastic identification strip is provided for each T-PAC. Any T-PAC may be plugged into any connector in the T-BLOC. The plastic identification strip is mounted in the particular position on the T-BLOC plugboard to correspond to its package location. Identifying symbols indicate the *logic* of the T-PAC. Color coding denotes the PAC type. Letters and numbers identify the *input* and *output* terminals.
5. T-PAC handles are correspondingly color coded for PAC identification.
6. A variety of service types of T-PACs are available to afford ease of implementation of the total system.

RELIABILITY

1. The proven reliability of the T-PAC family is attested to by the number of existing systems and the number of T-PACs employed in them. Specific references are available to bonafide inquirers.
2. Contributing factors to this high reliability are:
   a. Use of *high quality components* which in themselves have been designed for high reliability.
   b. Use of *proper de-rating factors on all parameters* affecting the operation of a component.
   c. Design for *worst case deterioration of rated characteristics* of components.
   d. *Quality workmanship.*
   e. An *active, rigorous,* and *authoritative* quality assurance and inspection program in the manufacturing process.
   f. MTBF probability data is maintained on a continuous basis as a final step in the program. *Continuous life testing* is conducted to provide empirical corroboration of the calculated data.

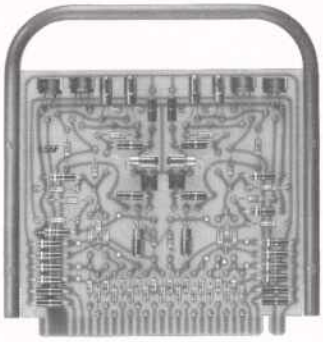
Logical Element
MODEL
LE-10



The *LE-10* is the basic unit in a T-PAC system. It is a *dynamic decision element* which performs logical functions in accordance with its plugboard connections. *ONE's* and *ZERO's* are represented by the *presence* and *absence* of pulses at the basic repetition rate of one megacycle.

The *LE-10* contains *four* (4) 4-input *AND* gates. Each gate input is available on the plugboard. The gate outputs are buffered into a 4-input *OR* structure, reshaped by a standard clock pulse, *amplified*, and made available at the bipolar outputs one microsecond after the input signals have occurred. Outputs are available as negative going pulses on the *ASSERTION* output and as positive going pulses on the *NEGATION* output. Each output terminal may be directly connected to its own PAC inputs or to the inputs of any other T-PAC.

Static Flip Flop
MODEL
FS-10



The *FS-10* contains two independent DC coupled flip flop circuits. Diode gated inputs to the *set* and *reset* side of each flip flop permit their use as logical elements. The *FS-10* is also useful as an *output* package in T-PAC systems where DC levels are required. *FS-10* outputs can be used as *relay drivers to energize sensitive relays* requiring up to 10 ma. drive. In shift register applications, the *FS-10* can shift at rates as high as *one megacycle*. No external carry delay between stages is required due to an inherent delay of the output relative to the input.

Internal diode steering guarantees that simultaneous drive to both sides of the flip flop will cause a change of state. The inputs are gated with the T-PAC one megacycle clock to

MODEL
FD-10 — *Dual Static Flip Flop*

This space is reserved for the forthcoming new FD-10 T-PAC. Tentative specifications for the FD-10 are as follows:

Serial Memory
MODEL
SM-10

The Serial Memory, *Model SM-10*, contains a *driver circuit, a magnetostrictive delay line*, and an *amplifier-reshaper*. It plugs into any connector of the T-BLOC. The adjacent position remains *unused* because of the double thickness of the package. The *SM-10* unit does not incorporate any logic. It is designed to be driven by a standard *LE-10 Logical Element* which furnishes *"write-in"* and *"erase"* control logic. The output driving capability of the *SM-10* is similar to that of the *LE-10 T-PAC* with both *ASSERTION* and *NEGATION* outputs provided. Storage capacities *up to 1500 bits* are available in a single *SM-10* unit. Greater loop storage capacity is obtained by cascading *SM-10* units. Any number may be cascaded providing an *LE-10* driver is used before each *SM-10*. Screw driver adjustment of $\pm 1\frac{1}{2}$ *microseconds* permits precise phasing of the delay setting. Temperature regulation is unnecessary over a

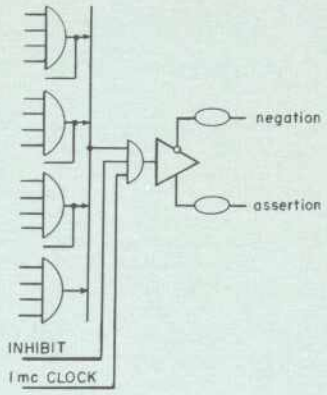
MODEL
WL-10 — *Word Memory*

The forthcoming new T-PAC one word line *Model WL-10* is similar in function to the serial Memory *SM-10*. The *WL-10* incorporates *gating logic, driver amplifier, magnetostrictive delay line*, and *amplifier-reshaper*, all integral within a single PAC. Delay lengths are manufactured to customer specifications within the range of *5 microseconds* to *40 microseconds*.

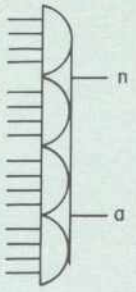
Additional logical flexibility is provided by an *INHIBIT* input which can be used to control *(ON-OFF)* the output of the gating structure. Three of the gate outputs are brought out to the plugboard. They may be jumpered together to form an 8-input or a 12-input gate.

SPECIFICATIONS

ASSERTION	
drive capability	20 T-PAC unit loads
amplitude	−4 volts
reference level	GND
NEGATION	
drive capability	40 T-PAC unit loads
amplitude	+4 volts
reference level	−1.5 volts
Output pulse widths	0.4 microseconds ±15% @ 10% level
Output impedance	91 ohms
Allowable input noise	0.5 volts
Power Requirement	−16 volts DC ±10% at 20 MA



LE-10 BLOCK DIAGRAM



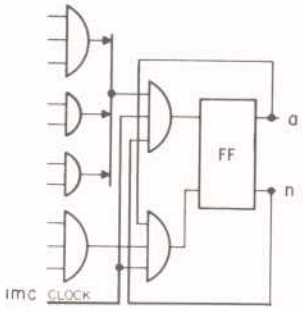
LE-10 LOGICAL SYMBOL

insure precise timing of the flip flop *cross-over* wave form. Cross-over *automatically* occurs between clock pulses.

The *FS-10* circuit layout is designed so that simple wiring changes can be made to modify the gating structures from *3 : 3-2-2* to *3 : 3-4* or *3 : 5-2* or *5 : 3-2* or *3 : 7*.

SPECIFICATIONS

Inputs	T-PAC LE-10 assertion and negation outputs or equivalent signals
Outputs	
ZERO level	−0.1 volts nominal
ONE level	−16 volts
Drive capability	Assertion and negation −20 T-PAC unit loads or 10 MA to −16 volts
Power Requirement	−16 volts DC ±10% at 27 MA



FS-10 BLOCK DIAGRAM
2 per PAC

FS-10 LOGICAL SYMBOL
2 per PAC

Two independent circuits per PAC
Gating logic approximately equivalent to the *FS-10* T-PAC
Output drive capability — ten or more T-PAC loads per output
Output level transition between clock pulses
Estimated cost — approximately $100.00

The *FD-10 Flip Flop* will require a positive supply voltage in addition to the standard −16 volts.

40°C temperature range.

SPECIFICATIONS

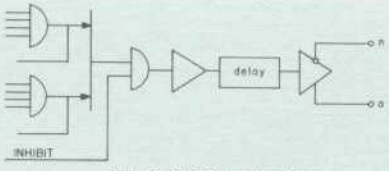
Input	
amplitude — nominal	+4 volts (LE-10 negation output)
minimum input amplitude	1.5 volts
maximum input amplitude	10.0 volts
reference level	−1.5 volts
input impedance	greater than 1,000 ohms
allowable noise	0.5 volts
NEGATION OUTPUT	
amplitude	+4.0 volts
impedance	91 ohms
reference level	−1.5 volts
drive capability	40 T-PAC unit loads
ASSERTION OUTPUT	
amplitude	−4.0 volts
impedance	91 ohms
reference level	Ground
drive capability	20 T-PAC unit loads
Power Requirement	−16 volts ±15% @ 60 ma. max.

SM-10 BLOCK DIAGRAM

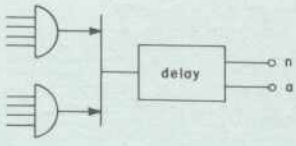
SM-10 LOGICAL DIAGRAM

The *WL-10* provides a compact convenient store for *one word buffers, address registers,* etc.

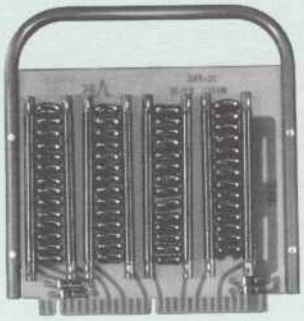
Screw driver adjustment of *± 1½ microseconds* provides precise, accurate and stable delay setting. Temperature range of operation is *0°C* to *+55°C*. The *WL-10* T-PACs may be cascaded *directly* to provide longer memories with multi-tap capabilities.



WL-10 BLOCK DIAGRAM



WL-10 LOGICAL SYMBOL

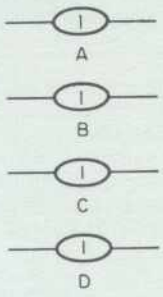


Unit Delay PAC
MODEL
DP-10

A T-PAC unit delay is a passive electrical delay of exactly one pulse period (one microsecond) and is used to provide *timing* or *delay* for the *ASSERTION* and *NEGATION* logical signals. The *DP-10* T-PAC is a single plug-in etched card which contains *four* individual one pulse period delay lines. The delay line *impedance* matches the *output* of the *LE-10*. These one pulse period delays may be used individually or wired in series by means of the T-BLOC plugboard connections. They afford an ideal method for implementing many logical functions such as *serial-to-parallel conversion* and vice versa, *short loop storage, frequency division, logical timing,* etc. Five unit delays may be wired in series directly. An *LE-10* T-PAC will provide *signal restoration* in place of a sixth unit delay for longer delay series.

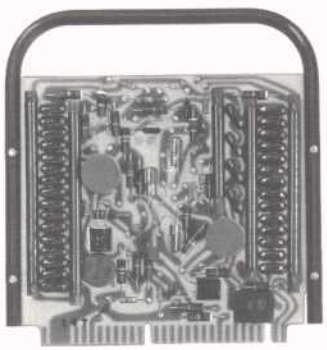
SPECIFICATIONS

Unit delay	1.00 microseconds ±2%
Impedance	91 ohms
Attenuation	less than 10% per microsecond
Cut-off frequency	5.6 megacycles
Number of unit delays per PAC	four
Power Requirements	none



DP-10 BLOCK DIAGRAM

Synchronous Generator
MODEL
TG-10

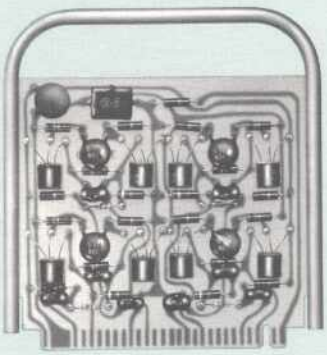


The purpose of the *Synchronous Generator* is to accept a *positive going, randomly-timed, arbitrarily shaped input pulse* such as might be obtained from a magnetic tape read amplifier, paper tape reader, keyboard, relay, switch, etc. and to convert it into one and *only one* properly timed and properly shaped pulse compatible with the standard T-PAC wave forms. The *TG-10* provides both *ASSERTION* and *NEGATION* outputs. Inputs to the *TG-10* are AC coupled internally.

SPECIFICATIONS

Input	
minimum amplitude	5 volts
maximum amplitude	20 volts
minimum pulse width	.25 microseconds

Thyraton Driver
MODEL
TO-10

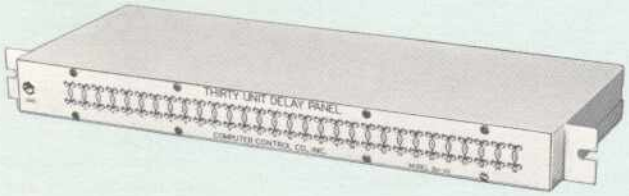


The *TO-10* contains *four* identical circuits mounted on a single PAC. Each circuit accepts standard T-PAC signals and generates output pulses of sufficient amplitude and width to provide reliable triggering of *thyratons* or *other devices* or circuits which cannot be driven directly by standard T-PAC signals. Conversion of the standard T-PAC signals to the specified *TO-10* output amplitude and duration is accomplished by a conventional one shot multivibrator circuit.

The *DU-10* contains 30 units of *passive electrical delay* identical to the delay units of the *DP-10*. It is intended for applications requiring a long series of electrical delay lines in either *straight* or *loop* form. The electrical delay lines are protected by the chassis enclosure. The *DU-10* affords a means of conserving package slots in a T-BLOC for utilization by active T-PACs. The electrical specifications of the delay lines are identical to those in the DP-10.

SPECIFICATIONS

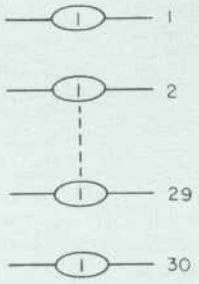
Unit delay	1.00 microseconds ±2%
Impedance	91 ohms
Attenuation	less than 10% per usec.
Cut-off frequency	5.6 megacycles
Number of unit delays	thirty
Dimensions	1¾" x 19" x 6¾"
Power requirement	none



30 Unit Delay Panel

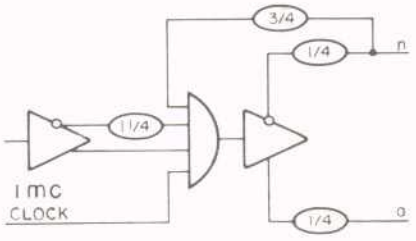
MODEL

DU-10



DU-10 BLOCK DIAGRAM

rise time	0.2 usec/volt or less
maximum pulse repetition rate	200 KC
maximum duty factor	50%
input impedance	5000 ohms maximum
maximum allowable noise	2 volts
Outputs	
ASSERTION	
amplitude	−4.0 volts nominal
reference level	GND
impedance	91 ohms
drive capability	20 T-PAC unit loads
NEGATION	
amplitude	+4.0 volts nominal
reference level	−1.5 volts
impedance	91 ohms
drive capability	20 T-PAC unit loads
Power requirement	−16 volts ±10% at 24 MA (at 100KC prf)

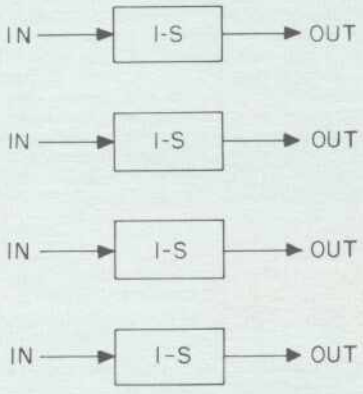


TG-10 BLOCK DIAGRAM

TG-10 LOGICAL SYMBOL

SPECIFICATIONS

Input	
minimum amplitude	+2.5 volts
minimum duration	0.4 microseconds
maximum amplitude	+16 volts
maximum allowable noise level	one volt
loading	3 T-PAC unit loads
Output	
amplitude	14 volts
duration	150 microseconds nominal
reference level	−16 volts
Power requirement	−16 volts at 18 MA



TO-10 BLOCK DIAGRAM

T-PACS

T-BLOC
MODEL
BL-10
BL-11

The *BL-10* T-BLOC has provision for 29 T-PACs plus a *TP-12 power supply*. All T-PACs including the power supply are inserted from the rear. A *retainer bar* which is quickly mounted and removed by means of knurled thumb screws provides *positive mechanical retention* and *protection* from shock and vibration. The front panel comprises a *taper pin plugboard* where all signals connections are made. Power and clock inputs for all the T-PACs are *pre-wired* and are *inaccessible* except by unscrewing and removing the top and bottom transverse bezels on the front of the T-BLOC.

Multi-colored plastic inserts indicate the T-BLOC plugboard connections and identify the type of T-PAC located in each slot. T-BLOCs are supplied complete with *taper pin insertion tool* and T-PAC *extraction tool.*

SPECIFICATIONS BL-10

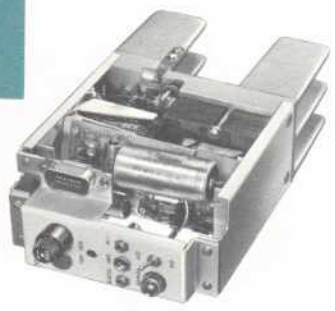
capacity	29 T-PACs plus TP-12 power supply
dimensions	5½″ high by 7″ deep and 19″ wide
color	3C beige
material	welded steel
finish	vinyl enamel on bonderized base

The *BL-11* is *identical* in size and most other respects to the *BL-10*. The major difference is that the space provided for the BL-10 plug-in power supply has been utilized to accept *three additional T-PACs* plus a *Master Oscillator* and/or *Slave Clock T-PAC*. It is intended for systems usage where the preference is for a common rack power supply in place of the individual plug-in modular supplies utilized in BL-10 systems. The *RP-10* power supply is offered for use with *BL-11* T-BLOCs.

SPECIFICATIONS BL-11

size	5½″ high by 19″ wide by 8″ overall depth
capacity	32 T-PACs plus an OC-10 or SC-10
color	3C beige
material	welded steel
finish	vinyl enamel on a bonderized base

Power Supply and Clock Driver
MODEL
TP-12



The *TP-12* supplies *DC power* and *clock drive* to the *29 T-PACs* in one T-BLOC, *Model BL-10*. The power supply circuit consists of a *stepdown isolation transformer*, a *full wave bridge rectifier*, and a *transistor regulator circuit* to maintain rated output voltage over a current range of no load to full load and over an input voltage range of 105 volts to 125 volts AC.

Included in the *TP-12* is the *clock driver circuit* which provides synchronous clock pulses to all the T-PACs in the *BL-10*. The *input* to the clock driver is obtained from the Master Oscillator, *Model MT-11*, which may be mounted in any one of the TP-12's used in a multi-bloc system. A recessed screw driver adjustment enables the clock pulse width to be adjusted.

The *TP-12* is plugged into the *BL-10 T-BLOC* from the rear. It is *locked* into position by means of a *spring clip*. The front panel contains a *power on-off switch, indicator light, slow blow fuse,* and *clock* and *power test points*. Aluminum cooling fins in the rear of the *TP-12* dissipate internally generated heat.

When specified, the *TP-12* will be supplied with the *MT-11* Master Oscillator factory installed and tested.

SPECIFICATIONS

input	105 to 125 volts, 60 cycles, 0.38 amperes maximum
output voltage	−15 to −17 volts under any combination of conditions of the specified input voltage, load current, and temperature ranges.
ambient temperature range	0°C to +55°C
clock drive capability	29 T-PAC clock inputs
physical dimensions	5″ high by 2½″ wide by 8½″ deep

Master Oscillator
MODEL
MT-11

The *MT-11* provides a precise source of synchronous clock pulses for up to *15 TP-12* clock driver circuits. The *MT-11* circuit consists of *a crystal controlled oscillator* and an *amplifier on an etched card submodule* that mounts inside any one *TP-12* in the system. A *width control* is provided for adjusting the output width.

The *MT-11* is rigidly mounted within the *TP-12*. Signal connections are made by means of *three taper pin leads.*

A special *MT-11* can be supplied for systems requiring more than 15 *BL-10's*. The special *MT-11* will drive up to 40 clock drivers.

SPECIFICATIONS

input	none required
output amplitude	+10 volts nominal
repetition rate	1,000 KC ±0.02%
output pulse width	0.26 microseconds at 10% amplitude
rise and fall times	.11 microseconds
reference level	−16 volts
power requirement	−16 volts DC ±10% at 19 MA

Power Supply

MODEL

RP-10

SPECIFICATIONS

input voltage	105-125 volts, 60 cycles
output voltage	−16 volts at 8 amperes
temperature coefficient	12 millivolts per °C
adjustment range	−13 to −19 volts
ripple	5 millivolts maximum
output internal impedance	.015 ohms
dimensions	5½″ high by 19″ wide by 11½″ deep

The *RP-10* is a *completely transistorized regulated 8 ampere power source* especially designed and conservatively rated for computer applications. It will provide power for *9 fully loaded BL-11 T-BLOCs*. A *voltmeter* and *ammeter* are provided to monitor output voltage and current. Full scale ranges are *25 volts* and *10 amperes* respectively. The output voltage is variable *±15%* from normal for marginal checking purposes. Provision is included for the optional addition of a second power supply to provide a supplementary voltage. This may be a *−90 volts DC supply* for neon indicators or some other voltage as required by the user.

Fuse protection is provided in both the *input* and *output* voltage circuits. An additional safety circuit is included which will blow the output fuse if the output *exceeds* 20 volts. This provides protection for the T-PAC transistors in the event of a malfunction in the *RP-10* of this nature.

The *RP-10* will supply −16 volt power for *320 LE-10's* operating at 1 mc continuously; *640 LE-10's* operating at a maximum duty cycle of 50%; *265 FS-10's;* or any combination which satisfies the relationship:

$.025\ \alpha\ N_{LE} + .03\ N_{FS} = 8$ amperes where α = maximum duty cycle at which the LE-10's will operate.

Master Oscillator

MODEL

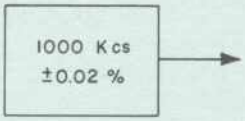
OC-10

The Master Oscillator, *Model OC-10*, is the modular equivalent of the submodular MT-11. It is intended for usage with *BL-11* T-BLOC systems. It provides *one megacycle clock pulses* via an integral slave clock circuit to its *BL-11* and synchronizing drive to up to *14 Model SC-10* Slave Clocks in the other *BL-11's* in a system.

The *OC-10* plugs into a six contact etched circuit connector located behind the control panel of the BL-11. The connector will accept either an *OC-10* or an *SC-10* Slave Clock T-PAC. Clock distribution from the *OC-10* or *SC-10* is pre-wired to the 32 T-PAC connectors in the *BL-11*.

SPECIFICATIONS

input	none
clock drive output amplitude	15 volts nominal
width (at 10% amplitude)	0.5 microseconds nominal
frequency	1,000 KC ±0.02%
power requirement	−16 volts DC ±10% at 25 MA



OC-10 BLOCK DIAGRAM

Slave Clock

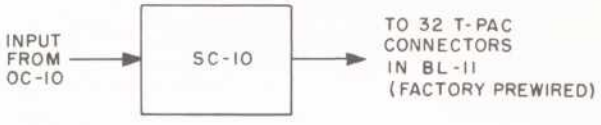
MODEL

SC-10

The SC-10 is a T-PAC similar to the OC-10 but without the crystal controlled oscillator components. It incorporates a fuse in series with the −16 volt supply to protect the T-BLOC. By-pass capacitors in the SC-10 filter high-frequency currents from the −16 volt supply bus. The SC-10 uses the same space in the BL-11 which is utilized by the OC-10. It duplicates in function the clock driver circuit contained in the TP-12 power supply.

SPECIFICATIONS

input amplitude	15 volts nominal
reference level	−16 volts
output amplitude	2.5 volts nominal
width	0.25 microseconds at 10% level
power requirement	−16 volts DC ±10% at 6 MA



SC-10 BLOCK DIAGRAM

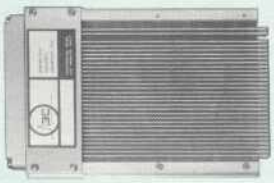
Unit Indicator
MODEL
UI-10

The *UI-10* will indicate the state of the output of the *LE-10* Logical Element or the *FS-10* Static Flip Flop. It also contains provision for driving a remote neon indicator in parallel with its own NE-2 lamp. Separate input terminals are provided for the *LE-10* and *FS-10* inputs.

SPECIFICATIONS

Input	
from an FS-10	−12 volts @ 0.2 MA
from an LE-10	1 megacycle pulse train @ −2.5 volts minimum
Power requirement	−90 volts @ 1 MA minimum to 2.3 MA maximum
Dimensions	13/32″ diameter X 2″ overall length
Maximum spacing	19/32″ on centers

PAC Extender
MODEL
XP-10

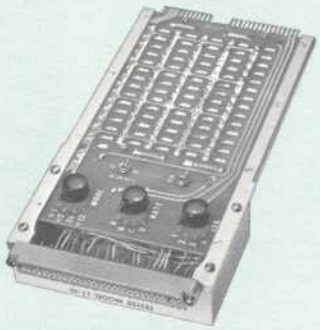


The function of the *PAC Extender* is to provide *unobstructed access* to any PAC while it is still electrically mounted in its appropriate T-BLOC Connector. The connector terminals on the front end of the XP-10 will mount into *any* T-BLOC connector and the connector on the rear of the XP-10 will accept the T-PAC which it is displacing. Front and rear terminals are directly *tied together* electrically.

Blank T-PAC
MODEL
ET-10

The blank T-PAC, *Model ET-10*, is a standard T-PAC card with *etched power* and *ground busses* from the appropriate connector terminals around its periphery. The bulk of the card is blank for the convenient mounting of *any* special circuits or components as desired by means of standard turret lugs and point-to-point wiring. *Drilling*, *lugging*, and *point-to-point* wiring of components and circuits do not require special skills and are easily performed.

LE-10 Tester
MODEL
LT-10



The *LT-10* plug-in PAC tester provides a complete testing facility for the *LE-10* Logical Element. It contains *a connector for the package to be tested, control switches, delay lines*, and *other components* mounted on a printed circuit card. Components and delay lines are protected from damage by a metallic and a lucite shield respectively.

The *LT-10* plugs into *any* T-BLOC connector. Tester insertion into the T-BLOC can be done without interfering with the T-BLOC plugboard wiring since the tester is inserted only to obtain power and clocking.

Four test modes selected by the appropriate switch provide a complete test for the *LE-10*. Both *dynamic* and *static* tests are built into the *LT-10*. Also tested are all germanium diodes. Test terminals are provided for waveform observation and performance monitoring by means of an external oscilloscope.

FS-10 PAC Tester
MODEL
FT-10

The *FT-10* plug-in PAC Tester provides a complete testing facility for the *FS-10* Static Flip Flop. It contains *control switches, a microammeter*, and *other components* mounted on an etched circuit card. *FT-10* insertion in a T-BLOC can be made into any connector without altering the T-BLOC plugboard wiring. The tester is plugged into the BLOC to obtain power and clocking only.

Both *static* and *dynamic* tests are provided. The tester also individually tests each germanium diode. Load switches provide independent loading on all *FS-10* outputs to permit testing under *worst loading* conditions. A *scope switch* individually selects each output for waveform observation.

Jumper Lead Set
MODEL
JL-10

QUANTITIES

2″ length	30 per color (except black) 75 black
4″ length	15 per color (except black)
6″ length	10 per color (except black)
9″ length	5 per color (except black)

The Jumper Lead Set, *Model JL-10*, contains 435 assorted lengths of taper pin jumper leads. The leads are made of plastic insulated #22 stranded wire with gold plated Amp taper pins. The assortment includes both solid colors and tracers for color coding. The colors are *red, blue, orange, white* and *red, white* and *blue, white* and *orange*, and *black*.

MODELS

PT-11, PT-12

T-PAC TESTERS

The cabinet mounted T-PAC Testers, *Models PT-11* and *PT-12*, are designed *for the bench testing* of all T-PACs in the T-PAC family. They are provided as a supplementary product for customers possessing unusually large quantities of T-PACs. The *PT-11* and *PT-12* Testers essentially duplicate the test equipment utilized by 3C in the final exhaustive testing of all T-PACs prior to shipment to our customers. *As such, they represent the ultimate in comprehensiveness.* The *PT-11* provides a variety of test modes for all T-PACs with the exception of the TCM Memory PACs. The *PT-12* duplicates the *PT-11* but also includes test facilities for TCM Memory PACs. *Additional information and prices are available upon request.*

Random Access Magnetic Core Memories

MODEL

TCM

A variety of *high-speed random access solid state magnetic core memories* are available for use with T-PAC systems. The 3C *Model TCM Memories* are directly compatible with T-PACs — both *physically* and *electrically*.

Design of the 3C random access *TCM Memory* is based on proven coincident current core storage techniques. The memory is intended for use with *any* type of digital system requiring *high-speed random access*. Word capacities *up to 4096* and word lengths *up to 40 bits/word* are readily assembled due to the flexibility of the modular construction employed. For systems requiring *more than 4096 words*, random access memories can be operated *in parallel* to achieve capacities *up to 16,384 words*. *High reliability* and *ease of maintenance* are featured. Access time to any address is as short *as 3.0 microseconds*. READ-WRITE cycle time between random address locations may be as short *as 6.0 microseconds*.

Manual control of operating voltages and currents is provided for marginal testing. The core planes and the power and control panel each have their own chassis. All other circuits are standardized and modularized on several basic T-PAC type of plug-ins. These PACs are combined in proper logical array to provide the following major functions of the 3C Memory system:

address register	x current drivers
information register	y current drivers
timing circuits	sense amplifiers
selection switches	inhibit drivers

Catalog TCM includes descriptions of the memory T-PACs and describes the read and write operating cycles. Copies of catalog TCM will be sent on request. Price and delivery quotations for specific memory configurations are also available on request.

PRICE LIST T-PAC
ONE MEGACYCLE, DYNAMIC, TRANSISTORIZED, PLUG-IN PRINTED CIRCUIT DIGITAL MODULES

MODEL	DESCRIPTION		UNIT PRICE	*QUANTITY DISCOUNT PRICE 5%
LE-10	Logical Element		$ 98.00	$ 93.10
FS-10	Static Flip-flop (2 circuits)		197.00	187.15
FD-10	Dual Static Flip-flop			
SM-10	T-PAC Serial Memory	19 to 100 microseconds	294.00	279.30
		101 to 700 microseconds	316.00	300.20
		701 to 1000 microseconds	352.00	334.40
		1001 to 1500 microseconds	385.00	365.75
		1501 to 2000 microseconds	427.00	405.65
WL-10	Word Memory		Price & Delivery information available April 15, 1961	
DP-10	Unit Delay T-PAC (4 delays per PAC)		64.00	60.80
DU-10	Thirty Unit Delay Chassis		515.00	489.25
TG-10	Synchronous Generator		143.00	135.85
TO-10	Thyratron Driver		98.00	93.10
BL-10	T-BLOC Chassis only (holds 29 PACs and power supply)		347.00	329.65
BL-11	T-BLOC Chassis only (holds 32 PACs)		373.00	354.35
TP-12	Power Supply with Clock Driver (for BL-10)		276.00	262.20
MT-11	Master Oscillator (for BL-10 and TP-12)		105.00	99.75
RP-10	Power Supply with rack mounting (for BL-11)		648.00	615.60
OC-10	Master Oscillator (for BL-11)		138.00	131.10
SC-10	Slave Clock (for BL-11)		71.00	67.45
UI-10	Unit Indicator		7.40	7.03
XP-10	PAC Extender		35.00	33.25
ET-10	Blank Panel with etched fingers and handle		9.60	9.12
LT-10	Logical Element Tester		387.00	367.65
FT-10	Static Flip-flop Tester		447.00	424.65
JL-10	Jumper Lead Set, 435 pieces of assorted lengths		43.00	40.85
PT-11	T-PAC Tester		Prices and Delivery on Request	
PT-12	T-PAC Tester			
TCM	Random Access Magnetic Core Memories			

effective date: March 15, 1961

PRICES: F.O.B. Framingham, Mass.
TERMS: Net 30 days
DELIVERY: From stock or as quoted

*Quantity Discounts are applied on basis of total price of individual orders.

Individual Order Total	Discount
$ 20,000.00 to $ 99,999.99	Less 5%
100,000.00 to 249,999.99	Less 8%
250,000.00 to 499,999.99	Less 10%
$500,000.00 and over	On request

This price list supersedes all previous price lists. All prices subject to change without notice.

No trade, O.E.M., educational, or other special discounts are available. 3C adheres rigidly to the policy of equally favored treatment to all customers.

All prices are domestic prices and are valid for U. S. A. and Canada and their territorial possessions. Add 10% for export shipments (except Canada).

Suggestions for ordering

Always order by catalog model number and name of product desired. Wherever possible, mention significant specifications to prevent misunderstanding- for example: *"T-BLOC, Model BL-10, 29 connectors, taper pin terminals."*

Orders may be sent to either Framingham, Massachusetts or Los Angeles, California.

To communicate with 3C

	Eastern Division	Western Division
Mail:	983 Concord Street Framingham, Mass.	2251 Barry Avenue Los Angeles, Calif.
Telephone:	CEdar 5-6220 (Boston) TRinity 5-6185 (Fram.)	GRanite 8-0481 BRadshaw 2-9135
TWX:	FRAM MASS 17	W LA CAL 6634

Western Union: *Direct telegram printer communications with Western Union are maintained for prompt handling of messages.*

Cable Address: Compcon, Framingham, Mass., U.S.A.

Shipments

Except when specified otherwise, shipments are generally made as follows:

(a) Under 20 pounds — Parcel Post

(b) 20 to 75 pounds — Railway Express

(c) Over 75 pounds — Truck or Carloading Company

For expedited service we will gladly ship by Air Freight, Air Express, Air Parcel Post, etc., as requested.

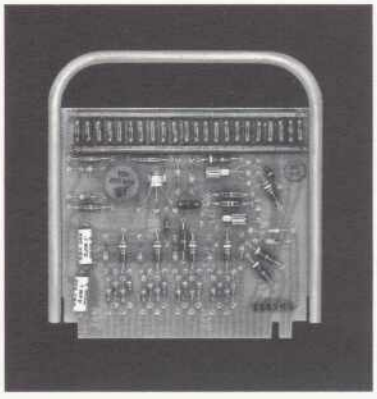
Standard warranty

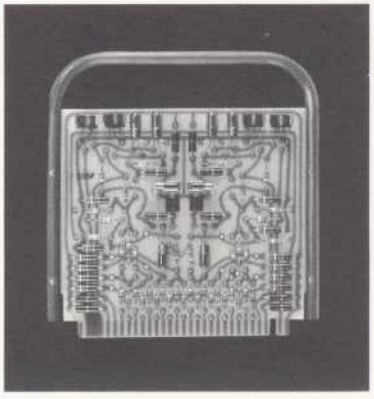
a) Computer Control Co., Inc., warrants all 3C products against defects in workmanship, materials, and construction under normal use and service for a period of ONE YEAR from the date of purchase except that liability for defective vacuum tubes, transistors, and germanium diodes shall conform and be limited to the obligations of the original manufacturer's warranties covering these components.

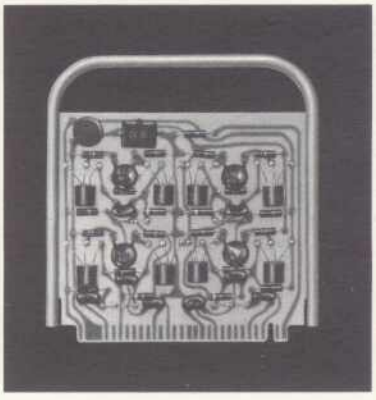
b) This warranty does not extend to any of our products which have been subjected to misuse, neglect, accident, or improper installation or application. Nor shall it extend to products which have been repaired or altered outside of our factory.

c) For service under this warranty, please advise the factory promptly of all pertinent details. Transportation charges covering return of defective products to our factory shall be at our expense if such products are determined to be defective within the limitations of this warranty. Computer Control Co., Inc. will repair or replace the defective product in accordance with its own best judgment.

d) Computer Control Co., Inc. requests immediate notification for any claims arising from damage in transit in order to determine if carrier responsibility exists.







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