SERIES

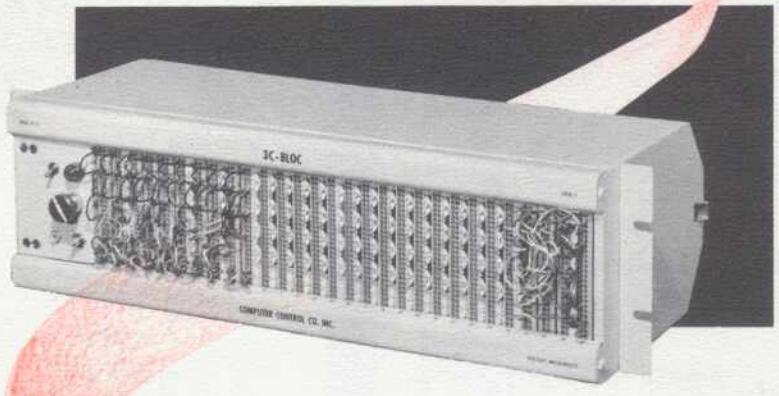
3C T PACs

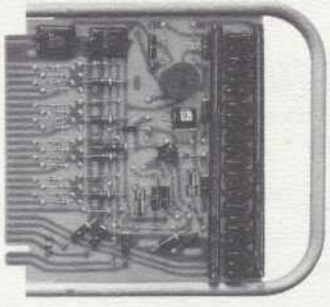
CATALOG T

descriptive information and
technical specifications
on the new

TRANSISTORIZED T-PAC ONE MEGACYCLE

DIGITAL MODULES





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contents

introduction . . .

High speed computing and digital control equipment can be implemented directly with the new Computer Control Company plug-in T-PACs, using the most advanced logical building block techniques. The T-PAC family of printed circuit, digital modules is fully transistorized. T-PACs operate at a one megacycle repetition rate and perform a comprehensive variety of operations and computations.

The compact T-PACs have been designed around basic LOGICAL ELEMENT package, model LE-10. The LOGICAL ELEMENT serves as the fundamental package type for any digital system. As evidence of its versatility, the LOGICAL ELEMENT can handle all 256 functions of three binary variables. It can perform 53,614 functions (82 percent) out of a total of 65,536 functions[1] of four binary variables, and many functions of five or more binary variables. In the language of the circuit designer, a single LOGICAL ELEMENT can serve any one of a variety of purposes, among which are the following:

amplifier
inverter
driver
buffer
flip-flop
counter stage
multiple-coincidence gate
frequency divider
half adder
shift register stage

LOGICAL ELEMENTS and other T-PACs, the various types of which are described in detail in another section, may be plugged into a chassis called the T-BLOC. By making the proper jumper connections on the plugboard format of the front panel of the T-BLOC, logical statements and system configurations can be quickly implemented.

Interchangeable plastic inserts are used to identify the terminals on the plugboard so that the logical representation of each T-PAC is recognizable at a glance. Taper pin solderless connectors assure clean electrical contacts that are positively maintained, yet readily rearranged.

T-PACs can be used in conjunction with commercially available input-output and storage devices to build installations ranging from small laboratory demonstrations and test set-ups to large scale digital control, computing, or data-processing systems. Circuit research, development and construction costs are bypassed. Experimental equipment, once used, need not be discarded, but may be used again in different applications merely by changing jumper connections on the T-BLOC plugboard.

The T-PAC family provides an ideal solution for permanent installations where reliability is of paramount importance. Extremely conservative operating margins have been obtained because it has been possible to concentrate engineering design and development on one basic circuit, that of the LOGICAL ELEMENT. Because of this concentration on one basic circuit, routine maintenance and repair time, as well as stocking of spare parts, are kept to a minimum. Any T-PAC can be replaced in just a few seconds.

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[1] 2^{2^n}, where n=4

general characteristics . . .

The design of the T-PAC family of digital modules is based upon the use of dynamic circuitry techniques first developed and applied to digital systems by the National Bureau of Standards[2] within the last decade.[3] The logical representation of the LOGICAL ELEMENT is shown in figure 1.

The gating configuration of figure 1 consists of a disjunctive combination of four four-variable conjunctions. Circuitwise, this corresponds to a group of four four-input AND gates which buffer together into an OR configuration. In addition, three of the four AND gates have their outputs accessible on the T-BLOC plugboard. These outputs may be jumpered together to obtain either an eight-input or a twelve-input AND gate. The overall gating configuration is the result of careful consideration. It was chosen as being the most suitable for the implementation of the widest variety

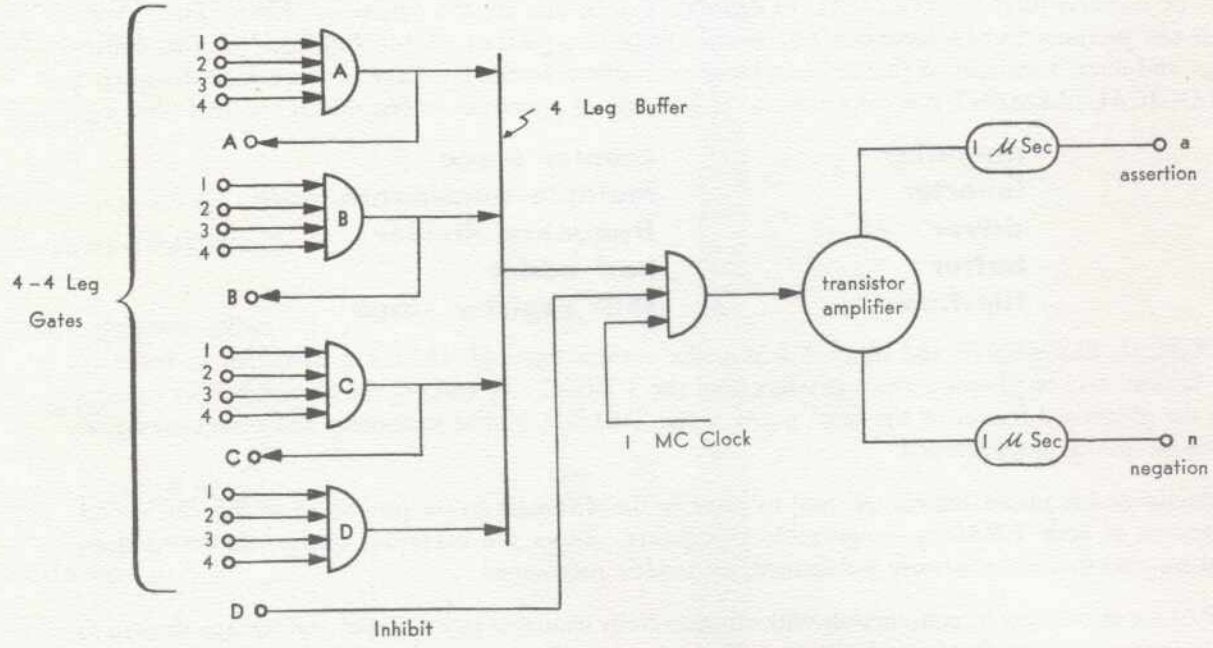


Figure 1. Logical Representation of LOGICAL ELEMENT, Model LE-10

of three, four and five variable binary functions, and also as being the most permissive to the minimization of these functions by means of the various mapping, chart and truth table methods currently in use by digital system designers.[4]

[2]The SEAC and DYSEAC computers, constructed by the National Bureau of Standards, were the forerunners of all the large digital computing systems which employ dynamic circuits. Computer Control Company has been using dynamic circuit techniques in its products and systems work since 1954.

[3]By comparison, the Eccles-Jordan bi-stable multivibrator or static flip-flop was first announced in print in *Radio Review, Vol. I, October 1919,* or nearly four decades ago.

[4]References:

Varnum, E. C. — "Binary Matrix Analysis of Relay Circuits," Machine Design, 1949
Veitch, E. W. — "A Chart Method for Simplifying Truth Functions," ACM Meeting, Pittsburgh, Pa., May, 1952
Karnaugh, M. — "The Map Method for Synthesis of Combinational Logic Circuits," AIEE Summer General Meeting, Atlantic City, N. J., June 1953
Brooks, R. W. — "Extension of the Veitch Chart Methods in Computer Design," ACM Meeting, Cambridge, Mass., Sept. 1953
Brooks, R. W. — "Symbolic Logic, Binary Calculation, and 3C-PACs," Printed and distributed by 3C
Engineering Staff 3C — "Logical Design of Digital Computing and Control Circuits with 3C PACs," Printed and distributed by 3C

significant features . . .

For the reader who may be unfamiliar with the concepts of dynamic circuits, following are listed some of the significant features of this relatively new technique, with particular reference to the T-PAC family of digital modules.

1) The dynamic circuit amplifier that is contained in the LOGICAL ELEMENT is a true pulse amplifier, with a relatively narrow bandwidth centered about a pulse repetition frequency of one megacycle.[5] (We use the term narrow as compared with the relatively wide bandwidth of an Eccles-Jordan static flip-flop.)

2) All T-PACs are synchronously operated with respect to the basic one-megacycle clock frequency. Synchronizing clock pulses are internally pre-wired to each package within the T-BLOC. The clock source is a crystal-controlled pulse oscillator contained in the plug-in power supply of the T-BLOC and may be considered as a supply voltage in nearly all respects.

3) By means of high fidelity electrical delay lines mounted within the LOGICAL ELEMENT both positive and negative outputs occur precisely one microsecond delayed from the input which generated them, and in synchronization with the clock output.

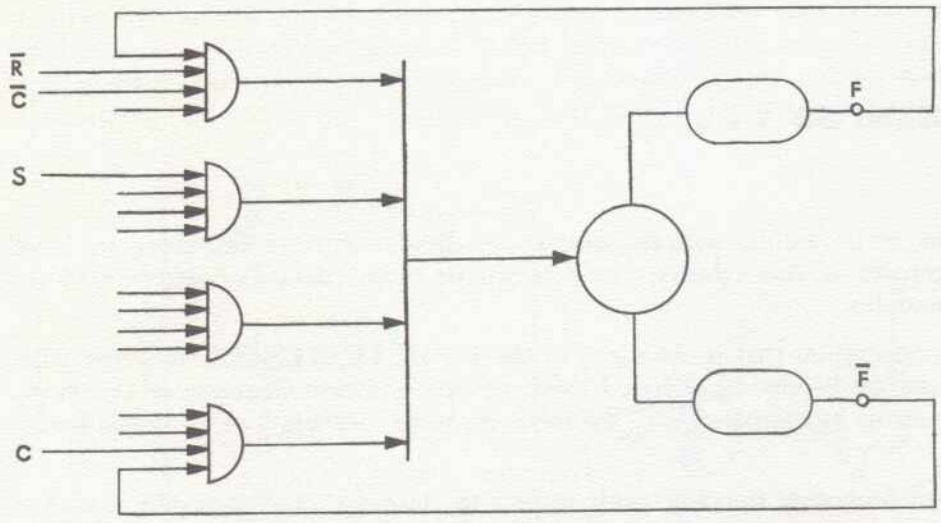
4) The diode gating configuration, or "decision-making" element, is internal to the LOGICAL ELEMENT module and constitutes the input part of the circuit.

[5]The term "dynamic" relates to the absence of d-c coupling in the amplifier and the consequent presence of pulse signals only throughout a system using dynamic circuits.

some of the advantages gained by using T-PACS . . .

A. *The LOGICAL ELEMENT Fulfills all Basic Logical Requirements.* Consider the following examples:

1. FLIP-FLOP. A flip-flop can be expressed as a binary function of three variables; i.e., the set, reset and complement inputs which determine the state of the flip-flop. Once the logical requirements are determined, the LOGICAL ELEMENT can be wired up as a flip-flop by making the proper plugboard connections. Figure 2 shows how this is done logically. This is only one form of flip-flop, however. Flip-flops can also be designed with the LOGICAL ELEMENT to provide precedance of binary over non-binary input or vice versa. Still others can be made exclusively binary or exclusively non-binary.



F = flip-flop output
S = set input
R̄ = reset input
C = complement input
C̄ = negation of complement input and is derived from the negation output of the LOGICAL ELEMENT which generates the complement function

Figure 2. The LOGICAL ELEMENT Wired as a Flip-Flop.

2. INVERTER. An inverter is a device which changes or reverses the polarity of its input signal. Logically, it negates or expresses the opposite value of the function which is its input. This capability is inherent in the LOGICAL ELEMENT because of the dual winding on the secondary of the pulse transformer in the amplifier circuit. This provides both polarities of the output signal. Hence, ASSERTION and NEGATION outputs are always available on each LOGICAL ELEMENT.

3. DRIVER. A driver circuit, such as a cathode-follower or emitter-follower is usually used in conjunction with the Eccles-Jordan circuits because the basic static flip-flop can drive only a small number of other circuits. In contrast to this, each of the two outputs of the LOGICAL ELEMENT can directly drive 20 inputs without intervening circuitry. Moreover, the interconnections between output and input are made with open wire jumpers rather than with coaxial cable despite the presence of one megacycle pulse trains. These very desirable properties are possible because the gain-bandwidth product of the LOGICAL ELEMENT amplifier contains a large gain factor and a small bandwidth

factor. The use of transistors plus a properly designed pulse transformer provide this gain in the form of current gain at the low impedance of 91 ohms at the output, without sacrificing signal level. Consequently, no additional driver circuits are required, and no capacitive cross-talk problems result from the open wire interconnections.

4. MULTIPLE-COINCIDENCE GATE. The primary decision-making elements of a digital system are the multiple-coincidence gates. Since a flexible and logically powerful diode gating array is an integral part of the LOGICAL ELEMENT, the addition of a multitude of special gating units to the list of T-PACs is not necessary.

5. OTHER USES. Single LOGICAL ELEMENTS can be used to implement other basic circuits such as half-adders, left-right shift register stages and binary counter stages. Groups of LOGICAL ELEMENTS can be used to swiftly implement sub-systems and complete systems such as arithmetic units, control units and data-processing systems.

B. *The Natural and Ideal Corollary to a Standard Package is a Standard Signal Waveform. The Waveform of the LOGICAL ELEMENT is Standard.* The LOGICAL ELEMENT waveform consists of a pulse of 3.0 volts amplitude, 0.4 microseconds width, and 0.15 microseconds rise and fall times.

The envelope to the pulse train is a function of the logical interconnections of the system and the input information to the system. It corresponds to the d-c waveforms of static or Eccles-Jordan circuits and is shown in figure 3.

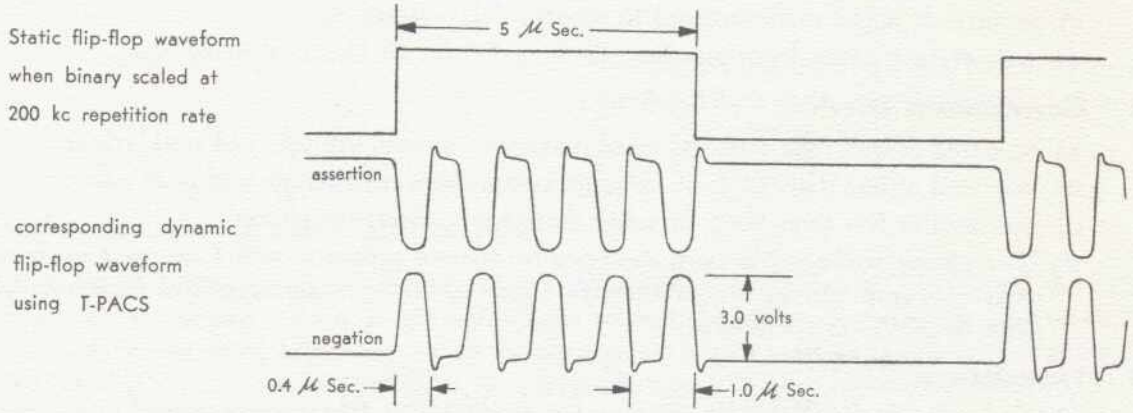


Figure 3. Comparison of Waveforms of Dynamic and Static Circuits

To assist the reader in orienting his thinking toward dynamic circuits, it can be pointed out that the pulse train waveform of figure 3 may be considered to be directly equivalent to the square wave of the static flip-flop. This is so because of the synchronous nature of the dynamic circuit. All actions automatically occur precisely at one microsecond intervals because of the timing control exercised by the internally-wired crystal-controlled clock. Since it is impossible for any operation to occur between pulses, it becomes academic that the waveform returns to the baseline instead of remaining a flat step. It would be equally academic if it were to go to infinity. However, the fact that the waveform is a pulse with a pre-defined shape, amplitude and timing is of considerably more than academic interest. The combination of standard package and standard waveform, which the LOGICAL ELEMENT provides, is of the greatest possible practical value to the system designer as well as to the maintenance personnel who will inherit the system.

reliability . . .

Long life and trouble-free performance have been designed into the T-PAC family. To this end, we have adhered rigidly to the following principles:

1. Use of high quality components, which in themselves have been designed for reliability.
2. Use of proper de-rating factors on all parameters affecting the operation of a component.
3. Design for deterioration of the rated characteristics of components.
4. Good workmanship.
5. Proper inspection and quality control.

The specific factors applied to the ratings and characteristics of components are as follows:

1. Resistors (composition)

a) operated at less than one half of the rated power dissipation.
b) 5% tolerance resistors used throughout while all circuits have been designed to operate with tolerance deviations in excess of 15%.

2. Electrical Delay Lines

a) 2% tolerance specified on all mica capacitors used in delay lines.
b) all mica capacitors operated well below 60% of rated operating voltage.
c) inductance sticks manufactured to ± 1% delay variation.
d) temperature dependency less than 60 ppm/°C for all electrical delay lines.

3. Germanium Diodes

a) operated at less than 50% of rated maximum inverse average and peak voltage.
b) operated at less than 50% of rated maximum forward average and peak current.
c) operated at less than 50% of rated maximum power dissipation.
d) The gating package has been designed to operate properly with a decrease in inverse resistance from rated specifications by a factor of 50 ; or an increase in forward resistance by 50% on all diodes.

4. Transistors

a) Surface barrier (SB102/2N345) and drift (2N247) transistors are used in all gating packages.
b) All transistors are operated well within their maximum ratings for power dissipations, collector voltage, and collector current.
c) Life test results indicate that the average life of the transistors used in the T-PACs should greatly exceed 30,000 hours.

5. Environmental Conditions

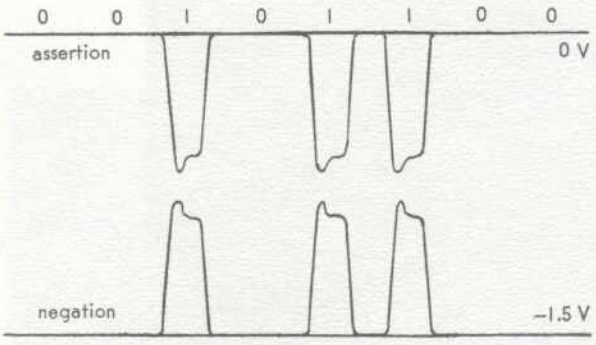
T-PACs have been designed to operate under usual conditions encountered in office, laboratory, or normal manufacturing area. No cooling is required within the ambient temperature range of −20°C to +55°C.

Computer Control Company, Inc., solicits your inquiries for special packaging modifications to meet abnormal environmental conditions.

description of the complete T-PAC family . . .

Logical Element, MODEL LE-10

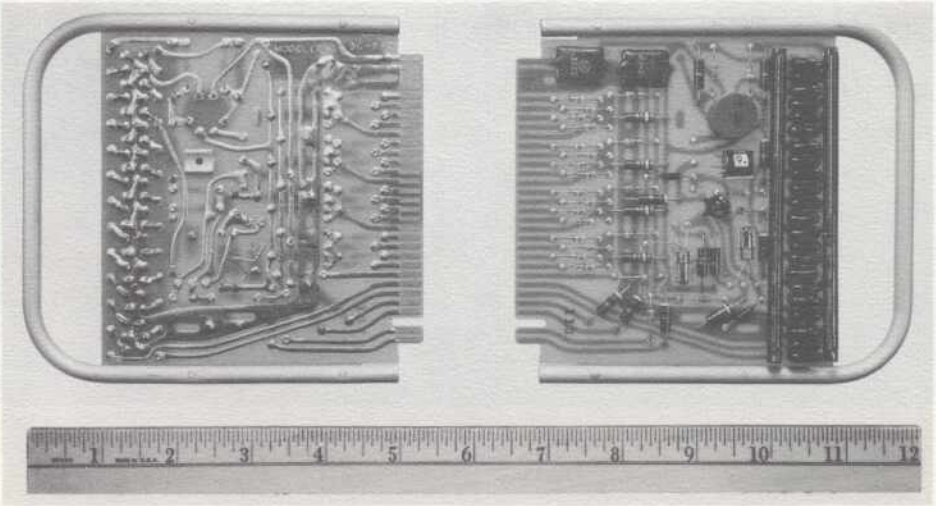
The basic LOGICAL ELEMENT has been described in some detail in the preceding sections. Figure 1 denotes its logical representation. It contains four four-leg gates, each leg being available on the T-BLOC plugboard. The gate outputs are mixed in a four-leg buffer, reshaped by a standard clock pulse, amplified, and made available one microsecond after the input signals have occurred. The LOGICAL ELEMENT output is presented on two separate lines — as negative pulses on the ASSERTION output and as positive pulses on the NEGATION output. Either output line may be directly connected via the T-BLOC plugboard to its own package inputs or to the inputs of any other T-PAC. Additional logical flexibility is provided by an INHIBIT input which can be used to control by a switch or other signals the output of the gating structure. Also, three of the gate outputs are brought out to the T-BLOC plugboard. By joining them together, an eight or a twelve input gate can be formed. All signals are defined by voltage ranges as follows:



Zero (or False) more positive than −0.5 volts
One (or True) more negative than −1.0 volts

The ASSERTION output of the LOGICAL ELEMENT is referenced to Ground through a 91 ohm termination resistor, i.e., it is normally Zero when the package is quiescent. The ONE State is denoted by the presence of negative polarity standard pulses whose baseline is at 0 volts or ground level. The NEGATION output is referenced to −1.5 volts through a 91 ohm termination resistor. The ONE State on this output is denoted by the presence of positive polarity standard pulses whose baseline is at −1.5 volts.

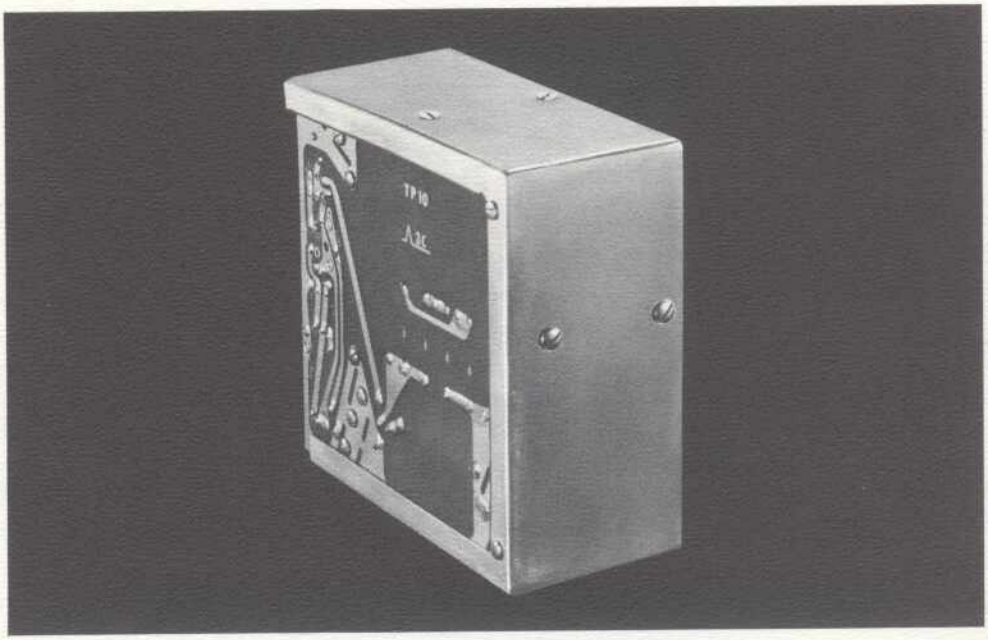
Basic dimensions of each T-PAC package type are 5″ by 5¼″.



plug-in power supply, MTP-10

The plug-in power supply is operated from 115 volts 60 cycles A. C. It provides –16 volts D.C. to all the T-PACs (total 29) used in the T-BLOC. This is the only voltage required by any of the T-PACs. The circuit comprises a step-down isolation transformer, a bridge rectifier, and a transistor regulator to maintain the output voltage at –16 volts over a current range of no load to full load and over an input voltage range of 100 volts to 125 volts A.C. The output voltage is variable by means of a recessed screw driver adjustment from –12 volts to –20 volts. Input power consumption is approximately 20 watts.

Integral with the power supply is the clock driver circuit which provides synchronizing clock pulses to all the T-PACs in the T-BLOC. The input to the clock driver is obtained from the master oscillator Model MT-10 which may be mounted in any one of the plug-in Power Supplies used in a multi-BLOC system.



master oscillator T-PAC, model MT-10

The Master Oscillator T-PAC provides a precise source of synchronizing clock pulses to any number of clock drivers up to a maximum of fifteen. (As mentioned previously, one clock driver is contained in each plug-in power supply.) The pulse repetition rate is 1000 ± 0.1 kilocycles. The circuit consists of a crystal-controlled oscillator and an amplifier on a single etched card that mounts inside the power supply package. In a multi-BLOC system, only one power supply unit need contain a Master Oscillator. All clock drivers will obtain their inputs from it.

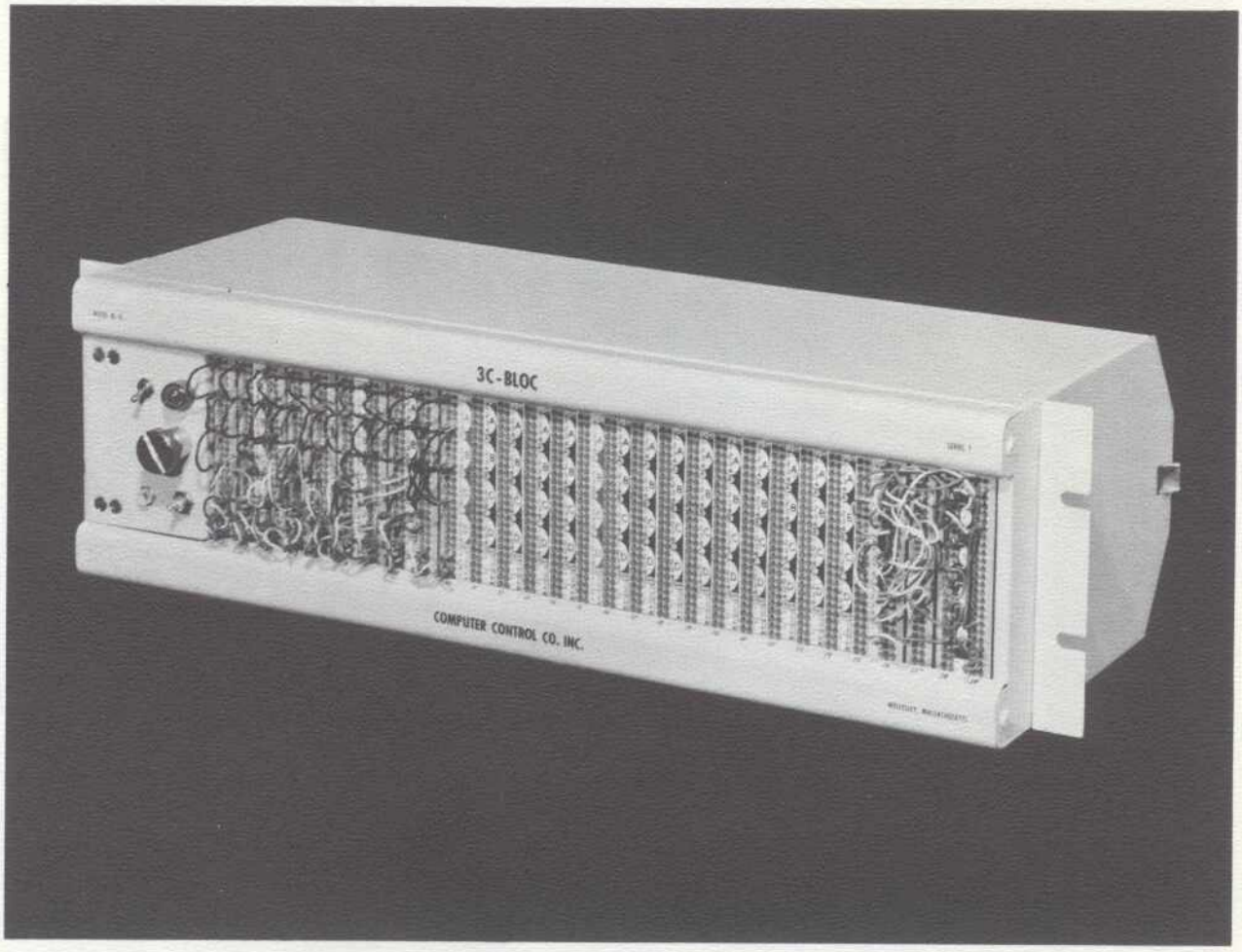
T-BLOC, model BL-10

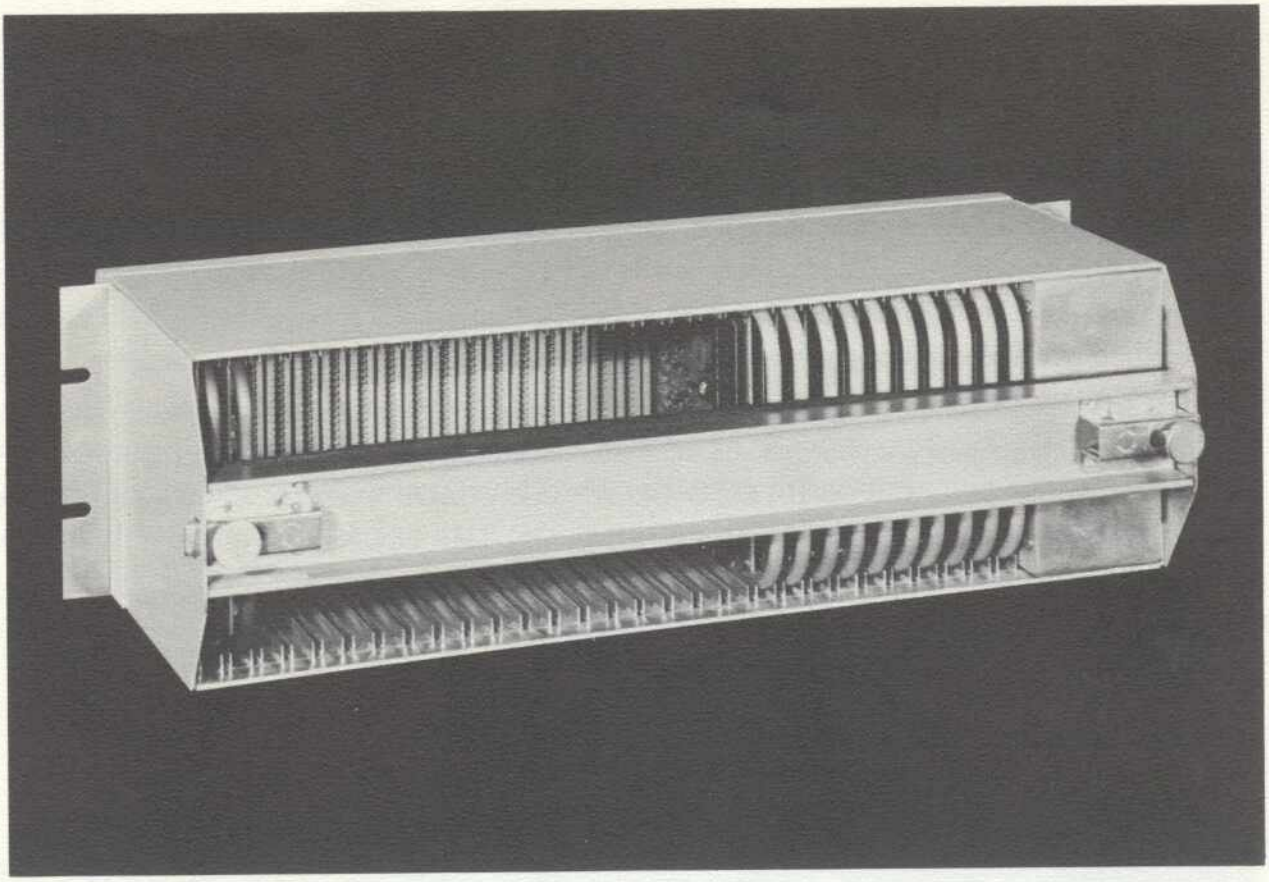
The T-BLOC, a chassis containing guide slots and connectors, has provision for housing twenty-nine plug-in packages of the T-PAC family in addition to a power supply package. All T-PACs are inserted from the rear. A hold-down bar which is quickly mounted and removed by means of knurled thumb screws provides positive mechanical retention and protection from shock and vibration.

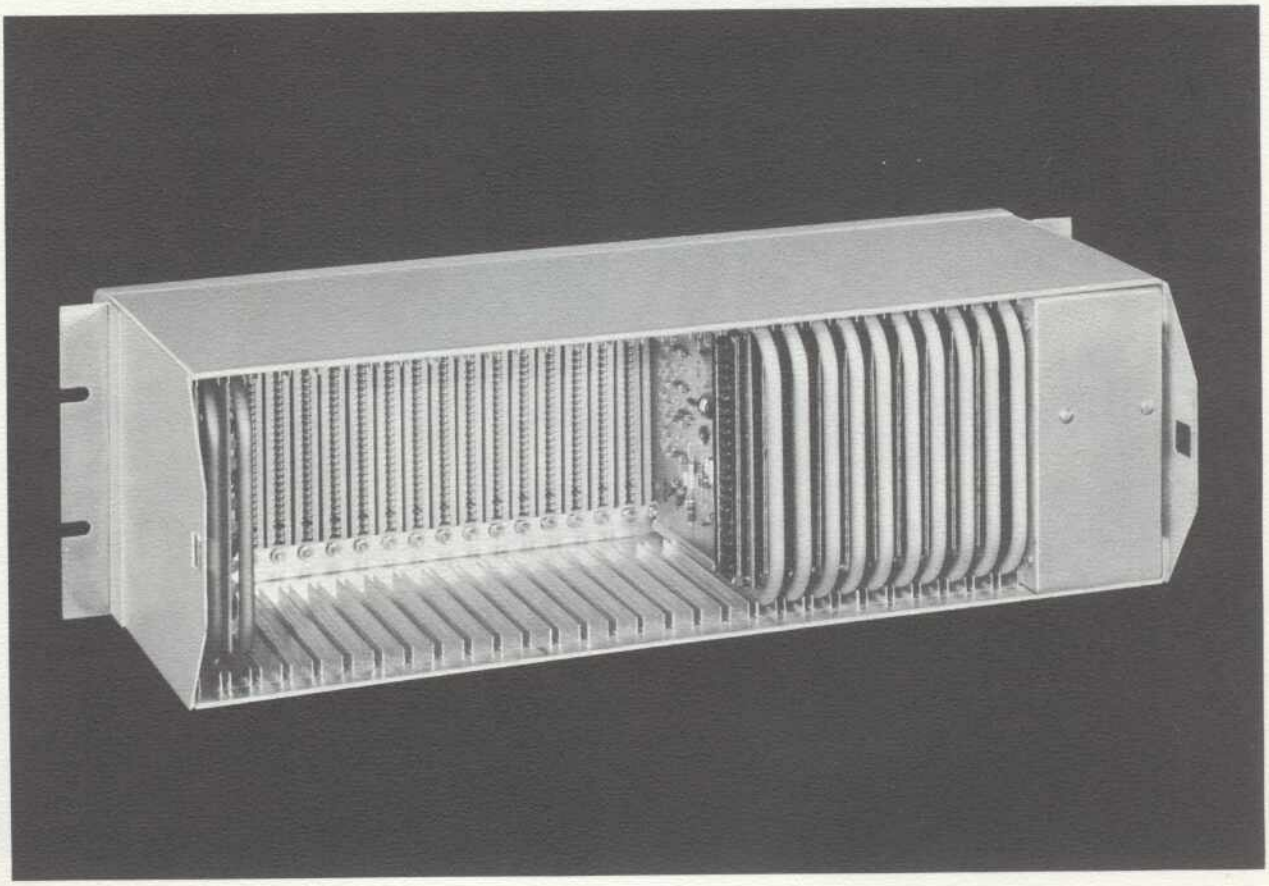
The front panel comprises a taper pin plugboard where all signal interconnections are made. Power and clocking inputs are prewired and are inaccessible except by unscrewing the front panel top and bottom bezels. IT IS IMPOSSIBLE TO DO ANY DAMAGE TO THE T-PACs OR THEIR COMPONENTS BY ANY FORM OF MIS-WIRING ON THE FRONT PANEL.

Multicolored plastic inserts identify the T-BLOC plugboard connections and also afford a convenient means of identifying different T-PAC usages within a system.

The T-BLOC, whose dimensions are 5¼" x 19" x 8" overall, occupies three audio units of standard rack space and is notched for standard rack mounting.







synchronous generator T-PAC, model TG-10

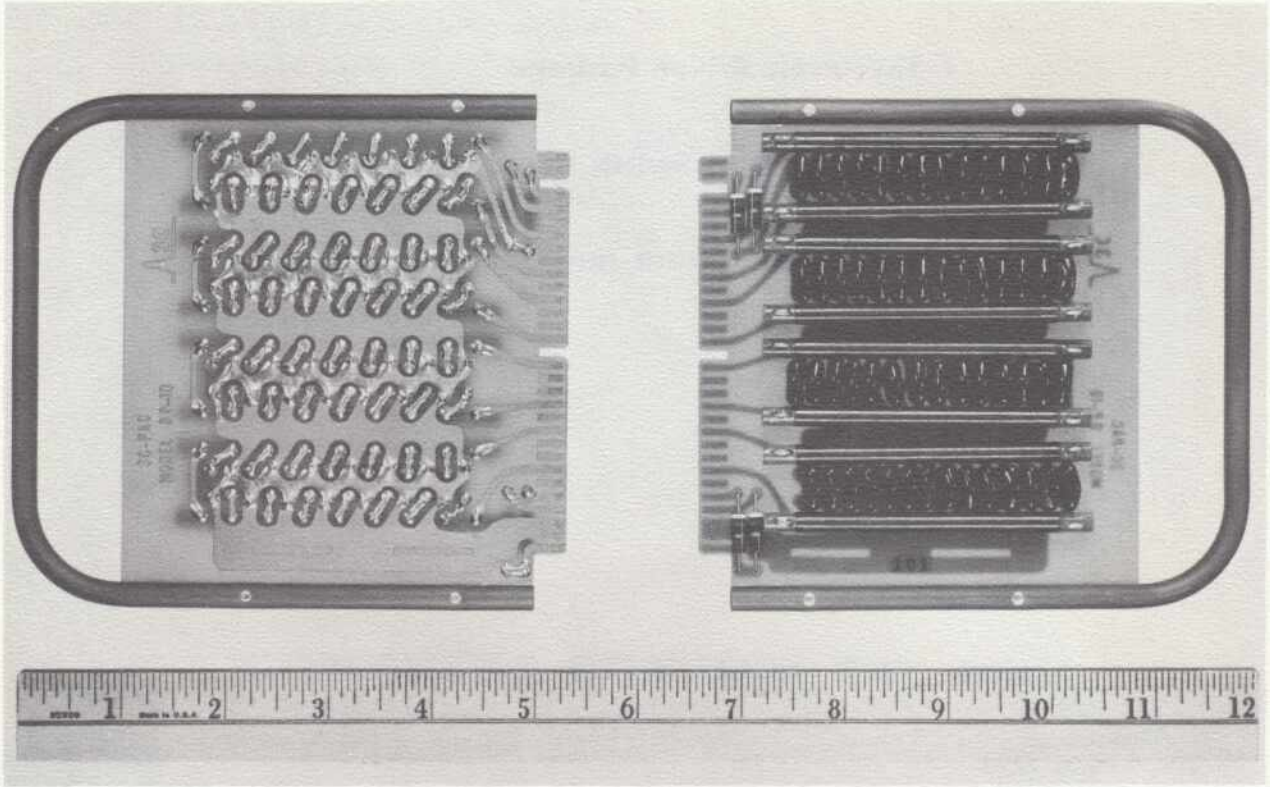
The purpose of the Synchronous Generator T-PAC is to accept a randomly-timed, arbitrarily-shaped input pulse, such as might be obtained from a magnetic tape read amplifier, a paper tape reader, a keyboard, relay, or switch, and to convert it into one and only one properly-timed and shaped pulse compatible with standard waveforms used in the T-PAC family.

The Synchronous Generator T-PAC is packaged similarly to the LOGICAL ELEMENT and can be inserted into any plug-in position of the T-BLOC. The appropriate plastic insert will then be used to identify the terminals of the Synchronous Generator. Assertion and negation outputs are provided similar to the LOGICAL ELEMENT.

unit delay T-PAC, model DP-10

The Unit Delay T-PAC contains four one-pulse period delay lines with a characteristic impedance of 91 ohms to match the outputs of the gating package. These one-pulse period delay lines may be used individually or jumpered in series by means of the T-BLOC plugboard connections. They can be used to fulfill a great many logical functions such as series-to-parallel conversion and vice versa, short loop storage, logical delays for timing and frequency division.

Delay length per unit delay is 1.00 microseconds $\pm$ 2%. Attenuation is less than 10% per microsecond. Cutoff frequency is 5.6 megacycles.



Under development and soon to be available are the following additional units of the T-PAC family:

- **Relay Driver Package**
- **Static Flip-Flop and Gate Package**
- **Delay Line Memory Package**
- **Thyratron Driver Package**
- **Indicator and Switch Panel**
- **Coincident current magnetic core memory**

COMPUTER CONTROL COMPANY, Inc.

PRICE LIST T

T-PAC Family of One-Megacycle Transistorized Plug-in Printed Circuit Digital Modules

MODEL	DESCRIPTION	UNIT PRICE	QUANTITY DISCOUNT PRICE *
LE-10	Logical Element T-PAC	$ 115.00	$ 109.25
TG-10	Synchronous Generator T-PAC	176.00	167.20
DP-10	Unit Delay T-PAC (4 delays per PAC)	64.00	60.80
MT-10	Master Oscillator Assembly	119.00	113.05
TP-10	Power Supply and Clock Driver	361.00	342.95
MTP-10	Power Supply with Master Oscillator MT-10 and Clock Driver	480.00	456.00
BL-10	T-BLOC Chassis, less: T-PACs and Power Supply	363.00	344.85
BL-10M	T-BLOC, Master Group, Complete with 29 ea. LE-10's 1 ea. MTP-10	4178.00	3969.10
BL-10S	T-BLOC, Driver Group, Complete with 29 ea. LE-10's 1 ea. TP-10	4059.00	3856.05
JL-10	One Complete Set of 435 Assorted Length Jumper Leads	79.00	75.05

Note: User can also fabricate leads to his own particular requirements using AMP taper pins and AMP crimp-on tool.

Prices: F.O.B. Wellesley, Massachusetts.

Terms: Net 30 days.

Delivery: From stock or as quoted.

*Quantity Discount Price: If an individual order on a unit price basis totals $20,000.00 or over, a 5% discount is applicable to the order.

All prices subject to change without notice.

This price list supersedes all previous lists.

October 30, 1957

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AVAILABILITY OF 3C SERVICES

Computer Control Company offers the services of its staff of logical designers, circuit designers, and systems engineers for your digital problems. Our complete flexibility permits a variety of workable arrangements to meet your special requirements. We will share your problems to whatever extent you desire. Our services range from minor consultation to complete design, development, and construction of your special purpose digital system. Write, wire, or phone us for further information.

WARRANTY. . .

The following standard warranty is applicable to all Series T 3C-PACs:

a) Computer Control Co., Inc. warrants all 3C products against defects in workmanship, materials, and construction under normal use and service for a period of ONE YEAR from the date of purchase except that liability for defective vacuum tubes, transistors, and germanium diodes shall conform and be limited to the obligations of the original manufacturer's warranties covering these components.

b) This warranty does not extend to any of our products which have been subjected to misuse, neglect, accident, or improper installation or application. Nor shall it extend to products which have been repaired or altered outside of our factory.

c) For service under this warranty, please advise the factory promptly of all pertinent details. Transportation charges covering return of defective products to our factory shall be at our expense if such products are determined to be defective within the limitations of this warranty. Computer Control Co., Inc. will repair or replace the defective product in accordance with its own best judgment.

d) Computer Control Co., Inc. requests immediate notification for any claims arising from damage in transit in order to determine if carrier responsibility exists.

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