COMPUTER CONTROL COMPANY, Inc.,
announces the addition of the products described in this brochure to its Series T family of transistorized dynamic digital modules.

This eight-page supplement forms a part of Catalog T titled *Descriptive Information and Technical Specifications on the New Transistorized T-PAC One-Megacycle Digital Modules.*

COMPUTER CONTROL CO., inc.

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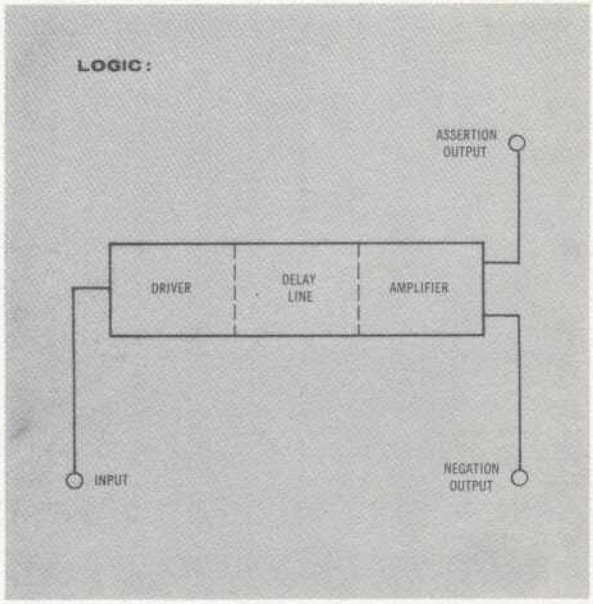
The SERIAL MEMORY unit, Model SM-10, consists of three basic sections; a driver circuit, a magneto-strictive delay line, and an amplifier circuit. The amplifier-driver section is mounted with the delay line to give a physically integrated package which plugs into one connector of the T-BLOC. In order to accommodate this package, the adjacent connector must be unused, since two connector spaces are required for each SM-10.

The SM-10 is simply a delay unit with amplifiers. It does not incorporate any logic. Its input is designed to be driven by a standard LE-10 Logical T-PAC or other logical circuitry with 'write-in' and 'erase' control exercised at this point. The output of the SM-10 is similar in load driving capability to an LE-10 package. Both assertion and negation outputs are provided.

Delays up to 560 microseconds are available in one SM-10 unit. Screwdriver adjustment of $\pm$ 1½ microseconds of delay allows final delay setting to be made quickly and easily. A small value of



SERIAL MEMORY

MODEL SM-10

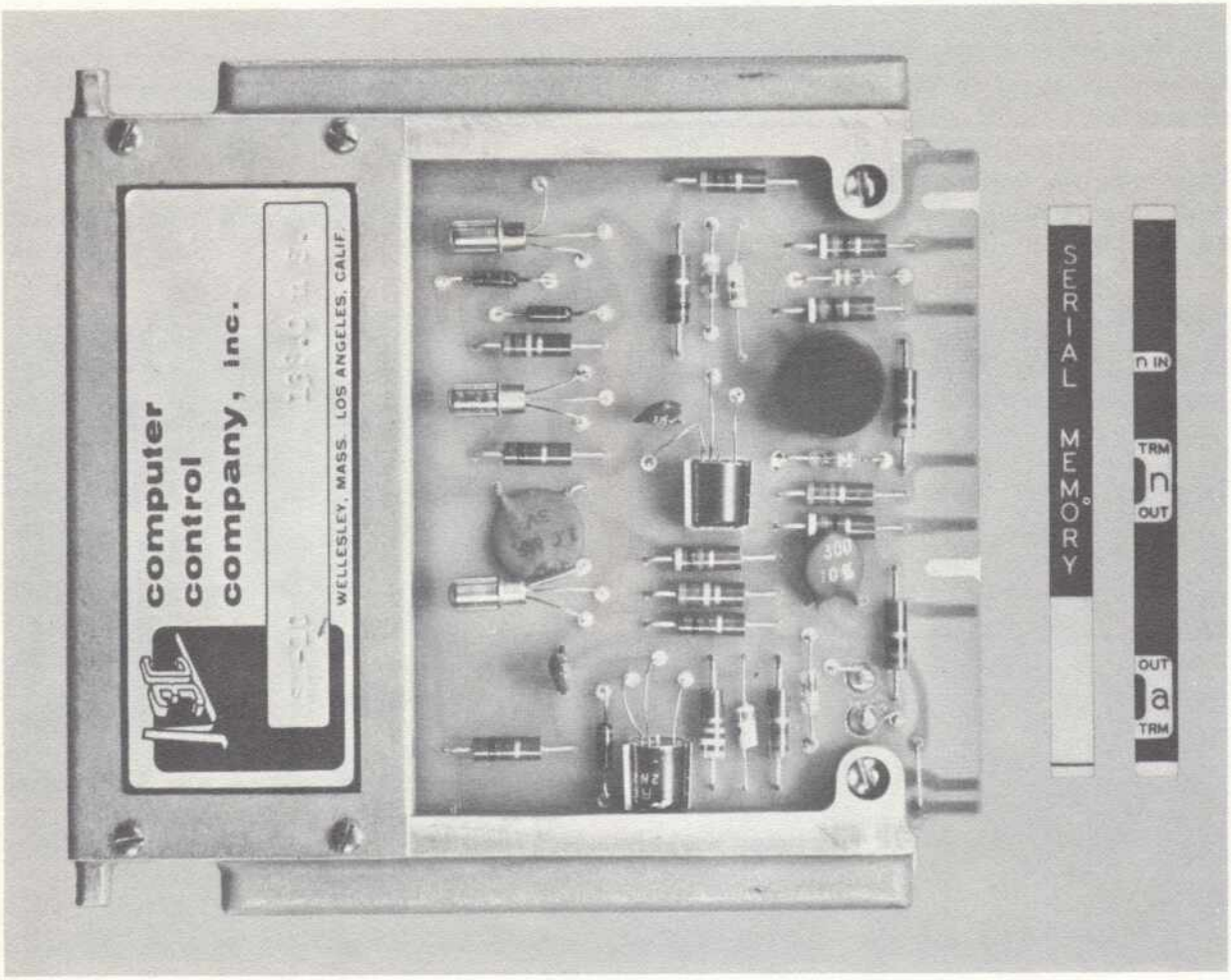
temperature coefficient of delay makes operation possible from 0 to 50°C or more, depending on length of delay, without use of temperature control. Special units utilizing even lower temperature coefficient of delay material are available for applications requiring greater temperature ranges. To obtain delays greater than 560 microseconds, it is necessary to cascade SM-10 units. Any number may be cascaded, provided an LE-10 T-PAC is utilized to drive each SM-10 unit.

Price:

QUANTITY	UNIT PRICE
1-9	$581.00
10-49	542.00
50-99	482.00
100-249	422.00
250-999	392.00

NOTE:

The prices listed are NET prices. Accordingly the standard T-PAC discount of 5 percent on single orders totalling $20,000.00 and over does NOT apply to the SM-10.



T-PAC STATIC FLIP-FLOP

MODEL FS-10

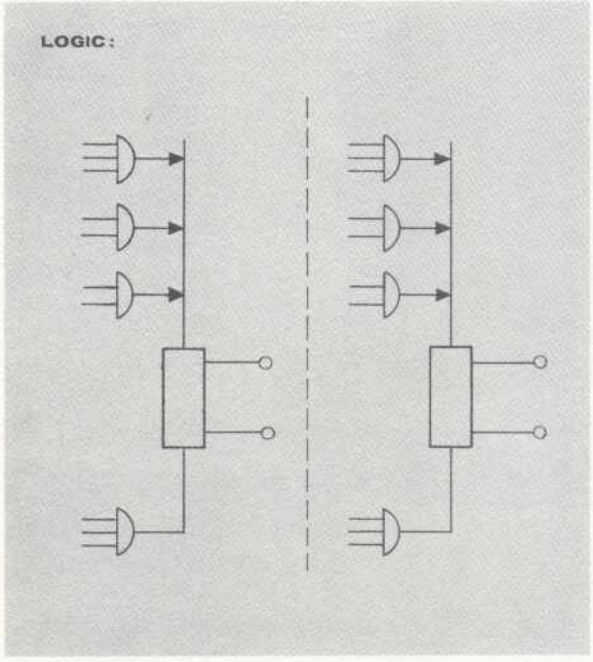
The T-PAC STATIC FLIP-FLOP, MODEL FS-10 contains two dc coupled Eccles-Jordan flip-flop circuits using surface barrier transistors. It may be used to implement a variety of functions. The diode gated inputs to the set and reset sides of the flip-flop permit its use as a standard logical element. It may be used as an output package in T-PAC dynamic systems where dc levels are required at the output terminals. Similarly, the FS-10 outputs can also be used as relay drivers to energize sensitive relays requiring up to 10 ma drive. In shift register applications the FS-10 can shift at rates in excess of one megacycle. No external carry delay between stages is required in this application due to an inherent delay in the output of 0.5 microseconds nominal. It is also directly useful for other standard flip-flop applications such as storage registers, output registers, etc.

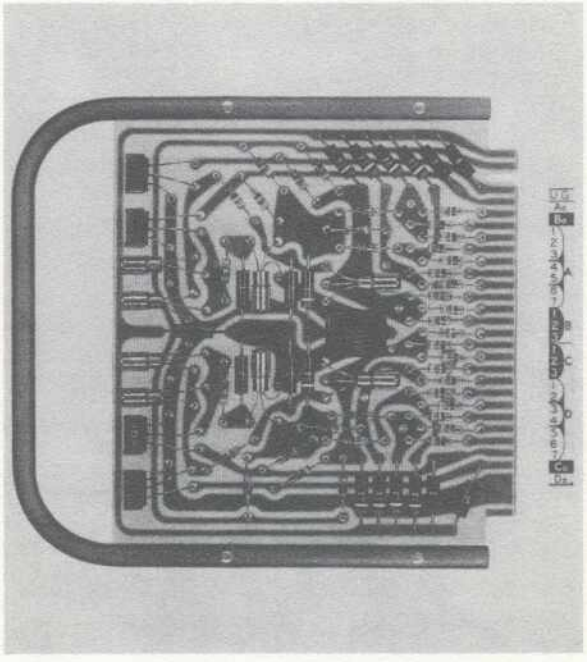
There are two independent circuits per card. Each circuit contains a flip-flop with gated inputs and amplified set and reset outputs. The maximum turn-over rate is in excess of one megacycle. The input gates accept normal T-PAC assertion and negation signals (or equivalent) and each output is capable of controlling thirty other gates. Output levels switch between −0.1 volts (ZERO) and −16 volts (ONE). When not driving gates, it is possible to drive external loads of up to 10 ma. Simultaneous drive to both sides of a flip-flop will complement or binary scale it. This is positively accomplished by internal cross-gating of the input signal within the flip-flop circuit. Also all inputs are gated with the T-PAC one-megacycle clock to maintain precise timing of the flip-flop cross-over waveform relative to the clock.

NOTE:
Etched circuit layout is designed so that simple wiring changes can be readily made to modify the gating structures from 3: 3-2-2 to 3: 3-4 or 3: 5-2 or 5: 3-2 or 3: 7.

Price: $197.00 per PAC
(two flip-flops)

LOGIC:



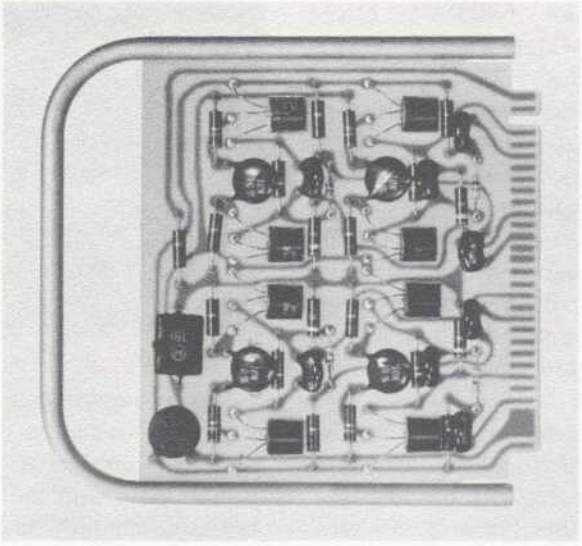


T-PAC THYRATRON DRIVER

MODEL TO-10

The THYRATRON DRIVER, Model T0-10, accepts standard T-PAC Model LE-10 signals. It generates output pulses of sufficient amplitude and width to provide reliable triggering of thyratrons or other devices or circuits which cannot be driven directly from the LE-10. Output amplitude is 14.0 volts positive. Duration of output pulse is 50 microseconds minimum and 75.0 microseconds nominal. Output impedance is 3.9K. Conversion of the half-microsecond LE-10 signals to the above specified amplitude and duration is accomplished by a conventional transistor one-shot multivibrator circuit. Four such independent circuits are contained on each Model T0-10, T-PAC.

Price: $98.00 per PAC
(four drivers)

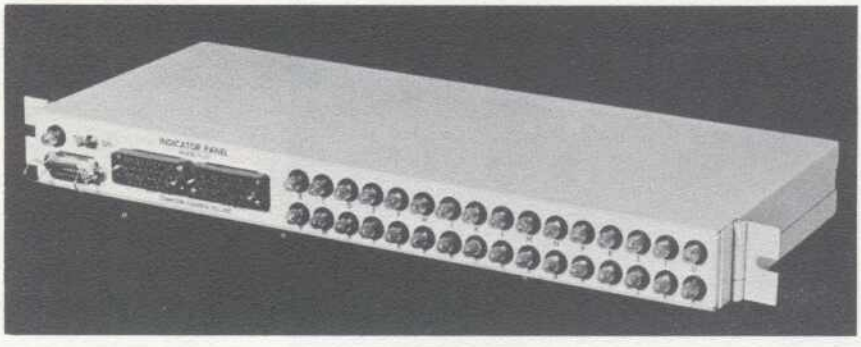


INDICATOR PANEL

MODEL TI-10

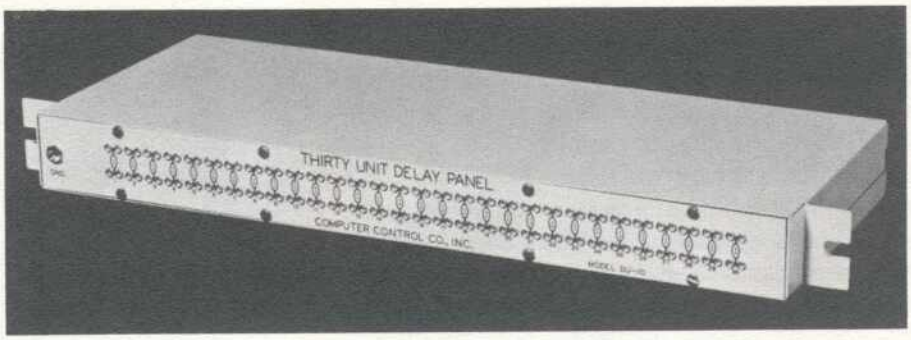
The INDICATOR PANEL, Model TI-10, provides visual neon indication of the state of the FS-10 static flip-flop or of the LE-10 logical element when wired as a dynamic flip-flop. The TI-10 chassis contains 32 neon indicators on its 19x1¾ inch front panel. The LE-10 outputs or the FS-10 outputs or any other signals which switch more negative than −4.0 volts may be brought in via taper pin interconnections to the input connector on the indicator panel up to a total of 32. Thirty two high voltage transistor amplifiers powered by a self-contained 90v transistorized power supply insure reliable operation of the neon indicators and also provide sufficient voltage drive on taper pin output jacks to drive remotely located neon indicators in addition to the self-contained indicators if desired. The Model TI-10 operates from 110v 60 cycle ac.

Price: $590.00



THIRTY UNIT DELAY CHASSIS

MODEL DU-10



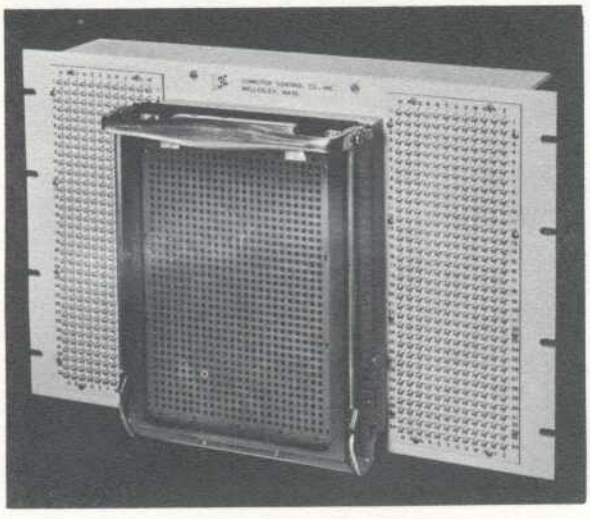
The THIRTY UNIT DELAY CHASSIS, Model DU-10, contains thirty separate electrical one-microsecond delay lines conveniently packaged in a standard 19x 1¾ inch rack mounting chassis. Each delay line is completely independent. The lines can be used separately or joined in series by simple taper pin jumper connections to form the desired total delay. The basic one-microsecond delay interval per line, accurate to within ±2 percent, can be used directly with the other Series T modules. Where large amounts of electrical delay are required in a minimum physical volume, the Model DU-10 affords an ideal solution. It is also useful for many other computer, test equipment, and pulse circuit applications. Waveshape of video and pulse information is accurately preserved by the high-fidelity M-derived lumped-constant delay lines. Upper cut-off frequency is 5.6 megacycles. Characteristic impedance is 91 ohms. Attenuation is 1 db per microsecond of delay.

Price: $560.00

PLUGBOARD PANEL

MODEL PB-10

The PLUGBOARD PANEL, Model PB-10 provides a simple and convenient means of obtaining an unusually large number of logical interconnections between T-PAC units. Units can be interchanged quickly from one configuration to another by replacement of the removable patch cord panel by another pre-patched panel. The Model PB-10 consists of one panel mounted AMP Universal Patchcord Programming System, containing 816 gold-plated contacts arranged in a 34x24 array. Each contact is brought out to a taper pin jack on the front terminal to permit convenient compatible wiring connections to the associated T-PAC terminals.



The Plugboard is center-mounted on a standard 19x12¼ inch rack panel. The taper pin jacks are arranged on either side of the plugboard with a direct 1:1 correspondence to the plugboard contacts to which they are internally wired. This wiring is covered by a protective housing on the back of the panel.

Price: $1270.00

Available Soon

A plug-in T-PAC tester package to completely test the operation of the Model LE-10 Logical Element T-PAC and its components including all diodes. The tester will plug in to any T-BLOC connector position and the T-PAC to be tested will plug into it in turn. Several testing modes will be provided to check all methods of usage of the LE-10 and to insure correct operation of all components.

Available on or about 1 Aug., 1958.

A coincident current random access magnetic core memory, featuring completely transistorized and modularized read, write, and address selection circuitry and complete compatibility with the other units of the Series T family of digital modules. The time required for a complete read/write cycle; i.e. access time, will be less than 10 microseconds. Word length and word capacity of the memory will be provided in accordance with specific customer requirements.

Available on or about 1 Sept., 1958.

Available on Request

Special T-PACs engineered to your exact specifications to meet your unique requirements whenever these cannot be implemented by our standard catalog items.

WARRANTY

a) Computer Control Co., Inc. warrants all 3C products against defects in workmanship, materials, and construction under normal use and service for a period of ONE YEAR from the date of purchase except that liability for defective vacuum tubes, transistors, and germanium diodes shall conform and be limited to the obligations of the original manufacturer's warranties covering these components.

b) This warranty does not extend to any of our products which have been subjected to misuse, neglect, accident, or improper installation or application. Nor shall it extend to products which have been repaired or altered outside of our factory.

c) For service under this warranty, please advise the factory promptly of all details pertinent to the defectiveness. Transportation charges covering return of defective products to our factory shall be at our expense if such products are determined to be defective within the limitations of this warranty. Computer Control Co., Inc. will repair or replace the defective product in accordance with its own best judgment.

d) Computer Control Co., Inc. requests immediate notification for any claims arising from damage in transit in order to determine if carrier responsibility exists.

AVAILABILITY OF 3C SERVICES

Computer Control Co., Inc. offers the services of its staff of logical designers, circuit designers, and systems engineers for your digital problems. Our complete flexibility permits a variety of workable arrangements to meet your special requirements. We will share your problems to whatever extent you desire. Our services range from minor consultation to complete design, development, and construction of your special purpose digital system. Write, wire, or phone us for further information.

COMPUTER CONTROL CO., inc.
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